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An Economical Data Acquisition System for Measuring and Recording Multiple Channels of Information at High Rates

Thomas Kottke

ARL-TR-860 September 1995

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13. ABSTRACT *(Maximum 200 words)*

A data acquisition system is presented that allows multiple channels of information to be captured and stored at high rates. The modular architecture of this system allows the data collection capability to be tailored to specific scenarios by the straightforward addition or subtraction of standardized components. Each signal that is to be monitored is routed to a separate analog-to-digital conversion and storage board that adjusts the magnitude and baseline of the input analog signals, performs high-speed analog to digital conversions, and stores the conversion values in short-term random access memory. Each channel can acquire and record 2,048 data points of 8-bit data at sampling rates up to 5 MHz. The actions of the individual conversion and storage boards are coordinated by a centralized data acquisition and storage control module. Following the data acquisition process, a data transfer control module is used to orchestrate the transfer of the recorded information from the short-term random access memory to the hard drive of a personal computer for processing and long-term storage. This report provides all the technical information that is required to maintain, expand, or duplicate this apparatus.

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1. INTRODUCTION

An interesting quirk of the human personality is the perception that better usually equates to bigger or more. This is certainly the case for the experimental physicist. If a single-channel oscilloscope is good, then a dual-channel scope is better, while a four-channel scope is great, and what you really want is an open-ended data logging system with an almost unlimited capability and a full complement of bells and whistles. Of course the fly in the ointment is that big capability is a traveling companion of big price. It was the combination of the usual desire to think big mixed with the usual funding constraints that spawned this effort.

In particular, the Weapons Concepts Division (WCD) is currently investigating the merits of electromagnetic armor. The requirement for high currents at high voltages is being satisfied by a power supply consisting of multiple capacitors wired in a parallel configuration. Additional capacitors are added to this power supply as the human desire for more manifests itself in the perceived need for a greater current delivery capability. At last count, this power supply incorporated 32 such capacitors and already there are murmurs concerning the next upgrade. Considerations relating to both safety and science make it desirable to monitor the time evolution of the current pulse from the individual capacitors. Each capacitor is capable of delivering a lethal electric shock. Therefore, from a safety standpoint, it would be very advantageous to know the extent to which each capacitor has been discharged during an experiment before the power supply is approached by test personnel. Another safety consideration arises from the limited lifetime of these high-density capacitors. By monitoring the time evolution of their charge storage capability, it is hoped that catastrophic capacitor failures can be predicted and avoided. The power delivered by each capacitor is a function of the electrical current. Therefore, knowledge of the time profile of the current pulse from the power supply is an important parameter in the analysis of mechanisms associated with these experiments.

The desire to monitor the current profiles from the individual capacitors in this scenario generates a need for a data acquisition system with the following characteristics. Clearly, the data acquisition system must be capable of simultaneously recording data from a large number of channels. Moreover, the system should be readily expandable to satisfy future as well as current requirements. These criteria suggest an overall modular architecture that allows the data collection capability to be augmented by the addition of standardized components. The particulars of the electromagnetic armor studies necessitate data acquisition

rates as high as 4 MHz and data acquisition periods as long as 0.5 ms. And of course, the system must be affordable.

The requirements of high data acquisition rates from many data channels precludes the use of a centralized real-time data storage scheme. Rather, a modular format is again used that groups each channel's data acquisition components with localized data storage capabilities. These memory components serve to record only the data from the associated channel. The embodiment of this arrangement groups the data acquisition and storage components for each channel on a single printed circuit board. This modular circuit assembly not only provides the foundation for effortless capability enhancement but also reduces most system field repairs to a simple matter of circuit board removal and replacement.

The need for simultaneous acquisition of data from many channels is achieved using a centralized controller for data acquisition and storage. Thus, although each data acquisition and storage module is independent in the sense that it can obtain and store its own data, each of these modules relies on cues from a central data acquisition controller to know when data is to be acquired and where it is to be stored. It is in this way that the multitude of independent data acquisition modules is integrated to yield a coordinated data acquisition system.

In most experiments and tests, the acquisition of data is merely the first step. It is the subsequent analysis of this data that generally tells the story. Since personal computers (PCs) are ideally suited to data reduction and analysis, a means of transferring information from this data acquisition system to a PC is also provided. Once again, a centralized controller is used. Following the data acquisition process in which each module simultaneously obtains and records information, a centralized data transfer controller takes control of the system. This controller sequentially interrogates each data acquisition module and orchestrates the transfer of the stored data to a PC for processing and long-term storage. An added complication of experiments dealing with high voltages is the need to totally isolate personnel from all high potentials. This requirement is satisfied by transferring the information from the data acquisition system to a remote PC along nonconducting fiber optic cables.

The final and perhaps most stringent requirement is that this system be affordable. This is a difficult criteria to quantify. One metric of affordability is the price of a comparable commercially available system. Plug-in cards are available for PCs that provide two channels of data acquisition and storage at roughly $400 per channel. The total price for 32 channels of this type of data acquisition and the associated PCs

is approximately $15,000. This price does not provide for electrical isolation via optical fiber communication, and there is some question as to the feasibility of operating a large number of channels simultaneously. The bottom line price for a 32-channel system using the scheme presented in this report is less than $10,000. Ultimately, affordability must be judged by the user.

This report describes the data acquisition system's capabilities and performance specifications. Moreover, this report attempts to provide the reader with all the necessary technical information to maintain, expand, or even duplicate this apparatus. Therefore, schematic diagrams, operational descriptions, printed circuit board masks, and parts lists are provided for all the major module types. In addition to these hardware considerations, examples of required software drivers are also presented and deciphered. The author apologizes for the inevitable use of jargon. However, in an attempt to make the text more palatable, a list of frequently used abbreviations is provided.

2. DATA ACQUISITION SYSTEM HARDWARE

2.1 Hardware Overview. This data acquisition system has been designed using a modular format to produce an apparatus that is flexible and serviceable. Each of the modules will now be presented and described in detail. The first module to be considered is the analog-to-digital conversion and storage board (ADCSB). Each of these units can obtain and store data from a single input channel. These modules are ganged together to provide a multichannel data logging capability. The operation of the ADCSBs is coordinated by a centralized data acquisition and storage control board (DASCB) that notifies the ADCSBs when to take data and where to store it. A single DASCB can orchestrate the operation of up to eight ADCSBs. Following the data acquisition process, a data transfer control board (DTCB) takes charge of the ADCSBs to direct the transfer of data from the individual ADCSBs to a PC. Again, a single DTCB can manage up to eight ADCSBs.

For safety-related reasons, data is transferred from the data acquisition system to the PC along fiber optic cables. Such a communications medium requires an optical transmitter or receiver at the ends of each cable. An optical transmitter and receiver are built into the DTCB. A PC fiber optic communication board (PCFOCB) is used to provide the necessary optical transmitter and receiver capability on the PC end of the fiber optic cables.

The final module that will be presented is the analog-to-digital conversion calibration board (ADCCB). Each ADCSB incorporates an array of light-emitting diode (LED) indicators that denotes the state of the local data bus. This feature provides the potential for an internal calibration system that can be used to adjust the amplifiers that serve as the front end of each ADCSB. The DASCB that normally controls the data acquisition function of the ADCSBs is a "one-shot" controller that has been specifically designed to allow only a single set of data to be acquired. For data calibration purposes, a free-running data acquisition mode is desirable that allows data to be taken continuously. The ADCCB is a centralized data acquisition control board that allows the ADCSBs to continually acquire data and display this information on the LED indicators. For calibration purposes, the DASCB is temporarily replaced by an ADCCB.

Independent modules are of little value unless they can be integrated into a complete system. To aid in this process, the final piece of hardware that is presented is a motherboard that the various modules can be plugged into. This motherboard provides for the communication between the various modules, supplies the necessary power sources, and allows convenient user access to both intraboard and interboard signals.

2.2 Analog-to-Digital Conversion and Storage Module. As the name implies, this module performs a number of functions. In particular, it adjusts the magnitude and baseline of an input analog signal, performs high-speed analog-to-digital conversions, stores the conversion values in random access memory (RAM), and then outputs these values when requested. The electronic circuitry that performs these functions is now presented in detail. These circuits are displayed schematically in Figures 1 and 2. In the following discussion, references to specific details on these schematics will be italicized. This module is contained on a single printed circuit board. Edge connector pin assignments for this board are enumerated in Table 1 and presented graphically in Figure 3. Artwork for this printed circuit board is illustrated in Figures 4 and 5. A component parts and price list is included in Table 2.

The first task of the ADCSB is to condition the analog input signal to ensure that its values lie within the measurement range of the analog-to-digital converter (ADC). As configured, the ADC is capable of measuring voltages in the range from 0 to 5 V. In order to achieve maximum resolution, the analog input signals should span as much of the ADC's measurement range as possible. Therefore, signals that extend over a range of more than 5 V must be attenuated, while signals that span significantly less than a 5-V range will need to be amplified. Since the input analog signals may be bipolar, this circuitry must be capable of adjusting the baseline as well as the amplitude of the conditioned signal. Figure 1 schematically presents the circuitry that performs this function.

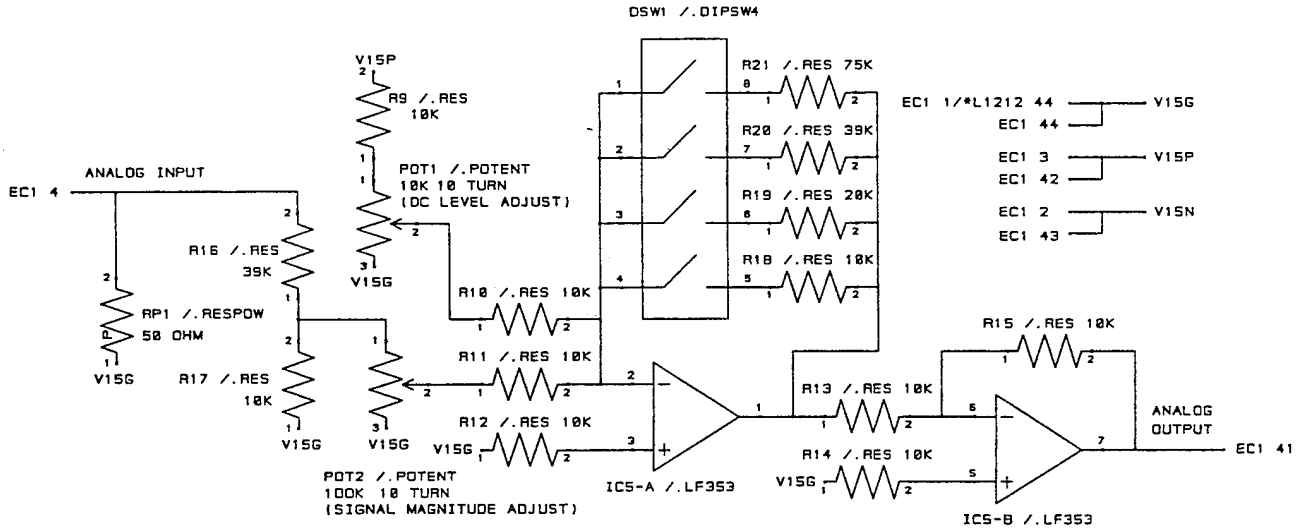

Figure 1. Electronic schematic of the A/D signal processing amplifier of the analog-to-digital conversion and storage board.

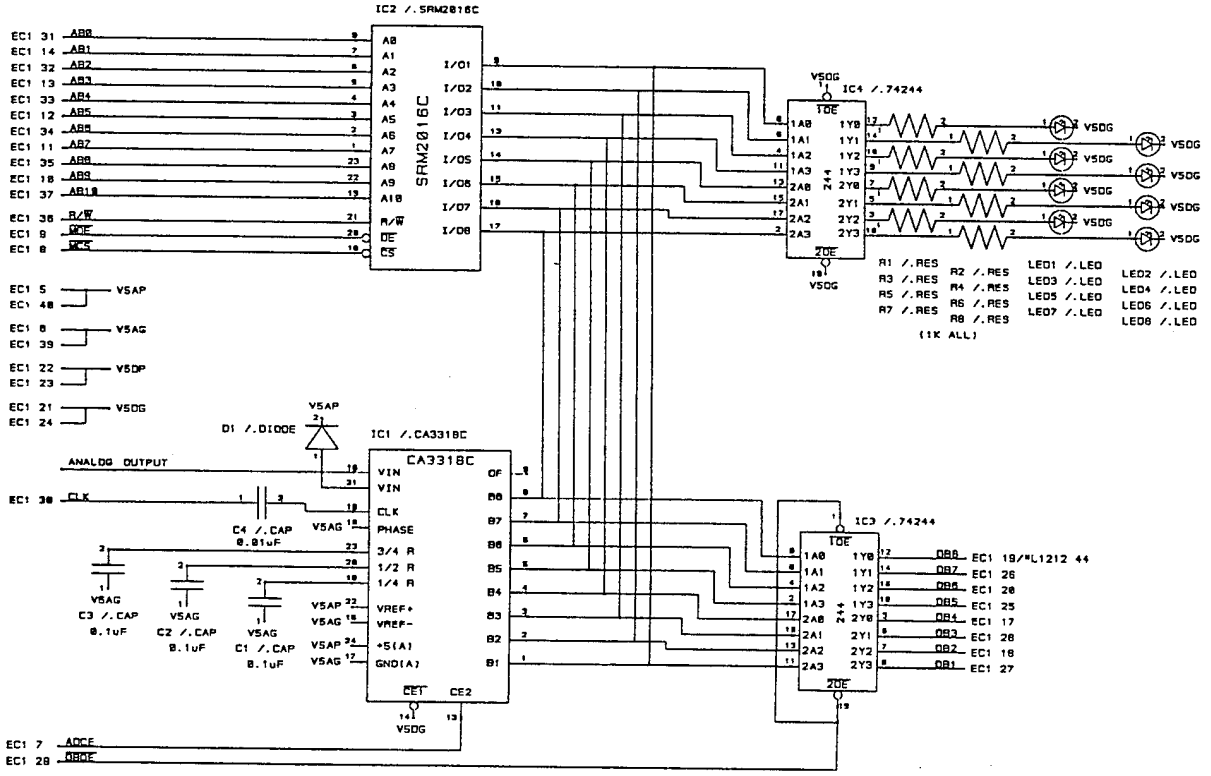

Figure 2. Electronic schematic of the A/D converter and short-term memory of the analog-to-digital conversion and storage board.

Table 1. Edge Connector Pin Assignments for the Analog-to-Digital Conversion and Storage Board

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V15G	2	V15N	3	V15P
4	AINPUT	5	V5AP	6	V5AG
7	ADCE	8	MCS	9	MOE
10	AB9	11	AB7	12	AB5
13	AB3	14	AB1	15	none
16	none	17	DB4	18	DB2
19	DB8	20	DB6	21	V5DG
22	V5DP	23	V5DP	24	V5DG
25	DB5	26	DB7	27	DB1
28	DB3	29	DBOE	30	none
31	AB0	32	AB2	33	AB4
34	AB6	35	AB8	36	R/W
37	AB10	38	CLK	39	V5AG
40	V5AP	41	AOUTPUT	42	V15P
43	V15N	44	V15G		

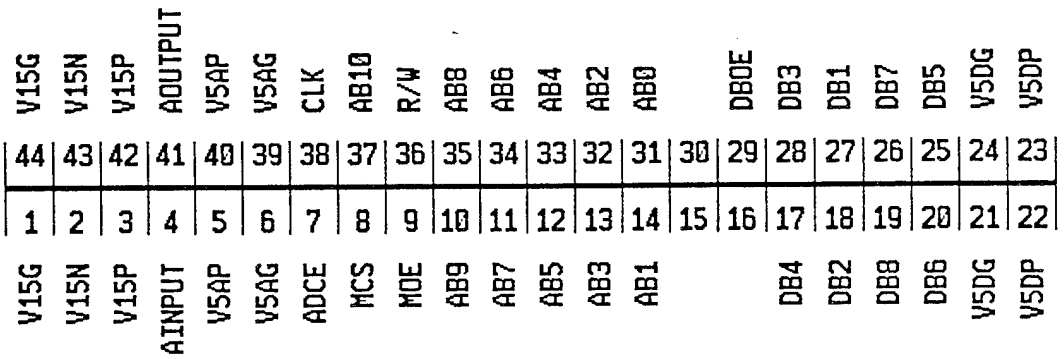

Figure 3. Edge connector pin assignments for the analog-to-digital conversion and storage board.

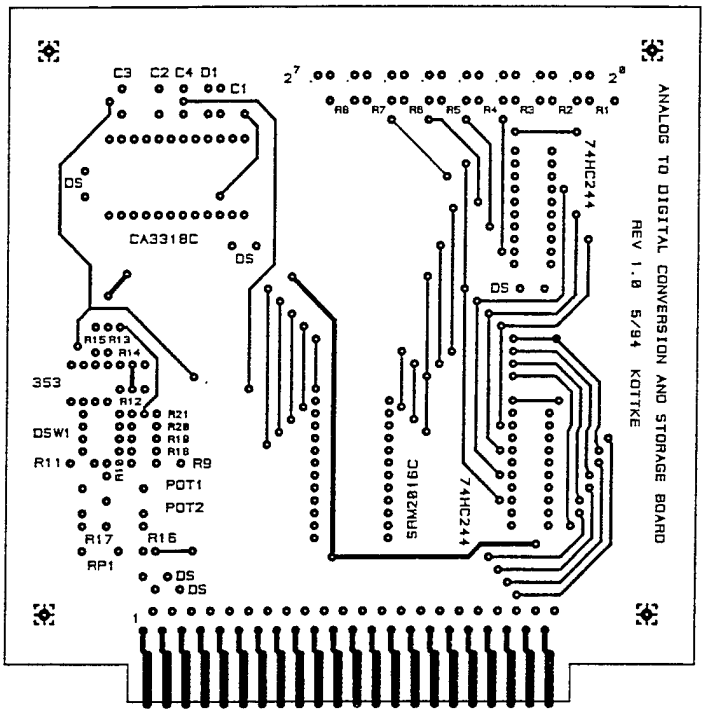

Figure 4. Artwork for the component side of the analog-to-digital conversion and storage board printed circuit board.

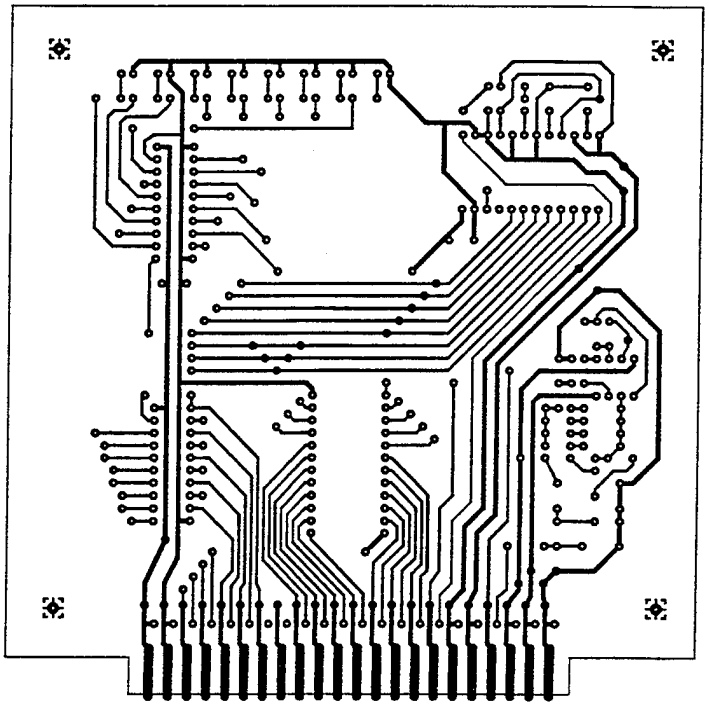

Figure 5. Artwork for the solder side of the analog-to-digital conversion and storage board printed circuit board.

Table 2. Parts List for the Analog-to-Digital Conversion and Storage Board

Description	Quantity	Part No.[a]	Cost
8-bit flash analog-to-digital conv.	1	CA3318CE-ND	26.87
16K(2K×8) CMOS static RAM	1	SRM2016C12-ND	4.88
74HC244 octal tristate buffer	2	MM74HC244N-ND	1.36
LF353 dual Bi-Fet operational amp.	1	LF353N-ND	1.14
0.1-μF ceramic capacitor	8	P4430	1.85
0.01-μF ceramic capacitor	1	P4424	0.11
high-efficiency rectifier	1	HER101	0.32
1-kΩ resistor	8	1.0KQ	0.48
10-kΩ resistor	9	10.0KX	0.99
20-kΩ resistor	1	20.0KX	0.11
39-kΩ resistor	2	39.2KX	0.22
75-kΩ resistor	1	75.0KX	0.11
50-Ω power resistor	1	SC3D50-ND	1.08
10-kΩ potentiometer	1	3006P-103-ND	1.41
100-kΩ potentiometer	1	3006P-104-ND	1.41
DIP switch, side-activated, 4-circuit	1	CT1944MST-ND	1.76
light-emitting diode, red	8	P367-ND	1.36
DIP socket, 8-pin	1	A9408-ND	0.40
DIP socket, 20-pin	2	A9420-ND	1.88
DIP socket, 24-pin, 0.600-in width	2	A9424-ND	2.26
edgeboard connector, 44-contact, 0.156-in centers	1	S5224-ND	3.48

[a] Part numbers are as listed in Digi-Key Catalog 941. Digi-Key Corporation, P.O. Box 667, Thief River Falls, MN 56701. Tel: (800) 344-4539, FAX: (218) 681-3380.

The analog signal that is to be conditioned, digitized, and stored is input at edge connector pin *EC1 4* as *ANALOG INPUT*. Resistor *RP1* can be connected to this input to match the input impedance of this board to the output impedance of the analog signal source. Overly large analog input signals can be decreased in magnitude by an appropriate choice of resistors *R16* and *R17*, that make up a constant value voltage divider. Potentiometer *POT2* is configured to provide additional adjustable signal magnitude reduction. This attenuated analog signal is then summed with a variable positive potential at the inverting input of an operational amplifier (op amp) that is configured as an inverting amplifier. The requirement for an adjustable baseline is satisfied by this summing capability. Potentiometer *POT1* controls the baseline level, while the value of resistor *R9* determines the range over which the baseline can be adjusted. The summing op amp *IC5-A* is also configured to amplify signals that may be small compared to the ADC's measurement range. Dual inline parallel (DIP) switch *DSW1* is connected to parallel feedback resistors *R18* through *R21* to provide amplification factors of approximately 1, 2, 4, and 8. The

combination of adjustable attenuation and amplification provides the user with a great deal of control over the magnitudes of the conditioned signals. Finally, since the summing and amplifying op amp acts to invert the polarity of the analog signal, an additional op amp *IC5-B* is included to reinvert the signal and provide additional buffering. The conditioned signal is available at edge connector pin *EC1 41* for external calibration and testing.

This conditioned signal is also routed to the remainder of the ADCSB module as *ANALOG OUTPUT*. The circuitry for this portion of the module is presented schematically in Figure 2. In particular, the conditioned signal is directed to the analog signal inputs *VIN* of the CA3318C ADC. This high-speed device can generate 8-bit conversions at sampling rates of up to 15 MHz.[1] The digital outputs from this ADC are interconnected to three additional components by a local data bus. Control of this data bus is regulated by selectively activating the four devices that are connected to it during the module's three modes of operation—data acquisition, data transfer, and calibration. Each of these modes of operation will now be considered in detail.

During the high-speed data acquisition process, analog signals are converted to equivalent digital values and stored in RAM in real time. Diode *D1* is placed between the *ANALOG OUTPUT* signal and the 5-V analog power supply potential to offer a measure of over-voltage protection for the CA3318C. This ADC is enabled through its two control lines, *CE1 bar* and *CE2*. To be enabled, the *CE1 bar* line must be grounded while the *CE2* line is held high. The *CE1 bar* line is, in fact, permanently connected to the ground of the digital power supply so the CA3318C is effectively controlled by the *CE2* line, which is accessed through edge connector *EC1 7* as signal *ADCE*. ADC conversion rates are determined by an external clock signal *CLK* which must be supplied on edge connector pin *EC1 38*.

Digital conversion values are stored on the ADCSB in an SRM2016C12 16-kilobit RAM chip. This device allows 2,048 8-bit words to be stored with an access time of 120 ns per word.[2] Control lines *CS bar* and *R/W bar* must be pulled low, via edge connectors *EC1 8* and *EC1 36*, for this chip to be enabled for data storage. External address signals *A0* through *A10* define the storage location of the digital ADC data which is input on lines *I/O1* through *I/O8*.

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[1] Harris Semiconductor Literature Department. Product Selection Guide. P.O. Box 883, MS CB1-28, Melbourne, FL 32901, 1990.

[2] S-MOS Systems, Inc. 1988/1989 CMOS Data Book. 2460 North First Street, San Jose, CA 95131, 1988.

Following the real-time data acquisition and storage process, the recorded information can be output to a central data storage facility for additional processing and presentation. In this mode, the data in the SRM2016C12 RAM chip is output through *IC3*, a 74244 octal tristate buffer, to a global data bus that is indirectly linked to the central storage device. It is assumed that many boards of this type may be transferring data at various times along this common global data bus. Therefore, access to this bus must be regulated to ensure that only a single board has control at any given time. Access to the global data bus is achieved by pulling both of the 74244 control lines *1OE bar* and *2OE bar* low via the *DBOE bar* signal at edge connector *EC1 29*.

With the data lines from the RAM chip connected to the global data bus, the contents of the SRM2016C12 are ready to be output. This memory device is configured for output by pulling the *R/W bar* control line high and the *OE bar* and *CS bar* control lines low via edge connectors *EC1 36*, *EC1 9*, and *EC1 8*. Address lines *A0* through *A10* are then used to step through the desired memory locations at a rate that is consistent with the data input rate of the transfer and central storage devices.

This module's final mode is used to calibrate the signal conditioning circuitry that was discussed previously. A second 74244 octal tristate buffer, designated *IC4*, is used to visually present the contents of the local data bus on an array of LEDs. The control lines of this 74244 are permanently grounded so this feature is always enabled. In practice, the *ANALOG INPUT* can be set to known potentials, while the baseline and magnitude control potentiometers are adjusted to output the desired ADC digital values as denoted by the LEDs.

In order to acquire, store, and retrieve data, this analog-to-digital conversion and storage module requires external address, clock, and control signals. The next section describes the module that provides these inputs and thus orchestrates the data acquisition and storage process.

2.3 Data Acquisition and Storage Control Module. This module orchestrates the operation of the previously described ADCSB during the data acquisition process. In fact, a single DASCB can oversee the operation of multiple ADCSBs. This module performs functions that include arming and triggering the acquisition process, providing control signals, and generating memory storage addresses. Figure 6 schematically displays the electronic circuitry that performs these operations. References to specific details

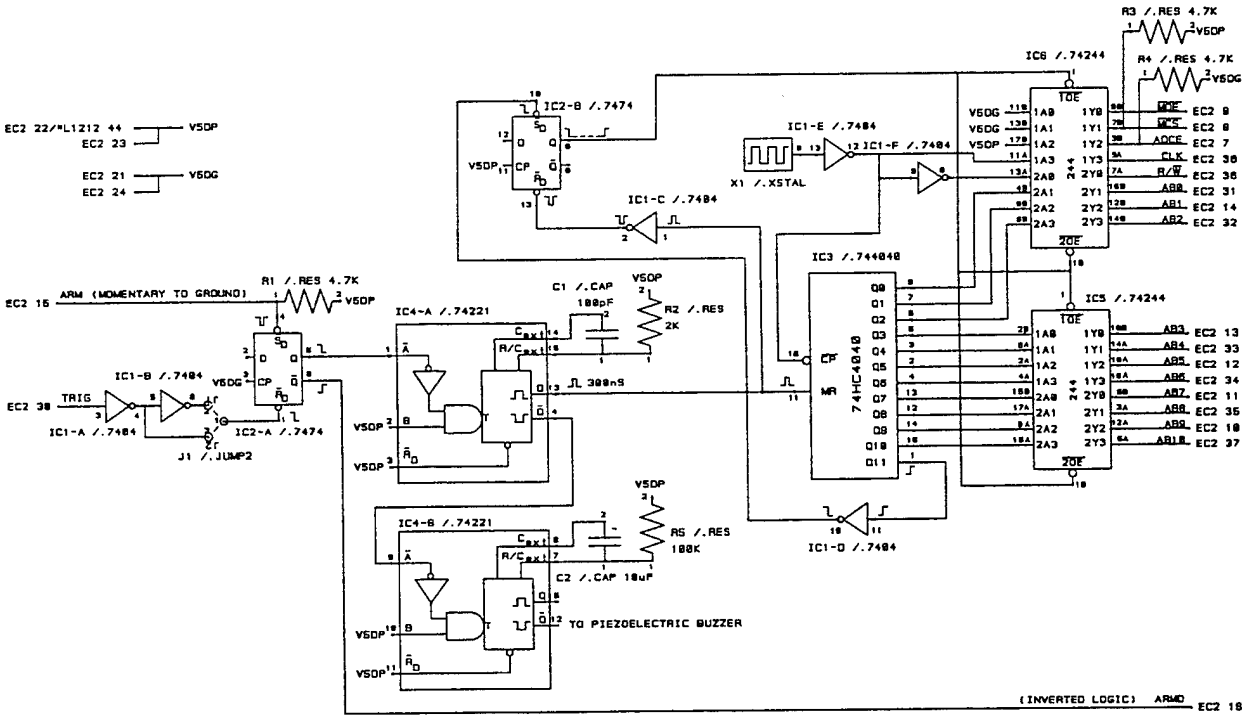

Figure 6. Electronic schematic of the data acquisition and storage control board.

on this schematic will be italicized in the following discussion. Table 3 contains a listing of the edge connector pin assignments which are also displayed graphically in Figure 7. Artwork for the printed circuit board is illustrated in Figures 8 and 9. A list of the required components and their prices is provided in Table 4. The arming and triggering processes will now be presented in detail.

An important consideration for the successful operation of this data acquisition system is that data be obtained only when the event of interest is taking place. This requires that the system be immune to pre-triggering and especially post-triggering. If the system were to accidentally pre-trigger, the operator might have the opportunity to detect this undesirable condition and rearm the apparatus. However, if the system post-triggers, then the previously acquired data of interest will be written over by the post-trigger event data. Pre-triggering and post-triggering are circumvented by the inclusion of a flip-flop in the arming and triggering circuitry.

The system is armed by momentarily grounding the *ARM* line that is accessed at edge connector pin *EC2 15*. This line is connected to the set pin S_D of the 7474 flip-flop *IC2-A*, which is normally held high

Table 3. Edge Connector Pin Assignments for the Data Acquisition and Storage Control Board

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	none	2	none	3	none
4	none	5	none	6	none
7	ADCE	8	MCS	9	MOE
10	AB9	11	AB7	12	AB5
13	AB3	14	AB1	15	ARM
16	ARMD	17	none	18	none
19	none	20	none	21	V5DG
22	V5DP	23	V5DP	24	V5DG
25	none	26	none	27	none
28	none	29	none	30	TRIG
31	AB0	32	AB2	33	AB4
34	AB6	35	AB8	36	R/W
37	AB10	38	CLK	39	none
40	none	41	none	42	none
43	none	44	none		

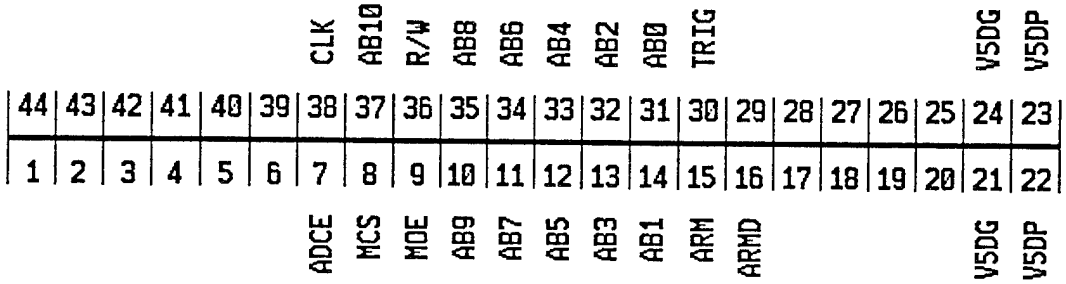

Figure 7. Edge connector pin assignments for the data acquisition and storage control board.

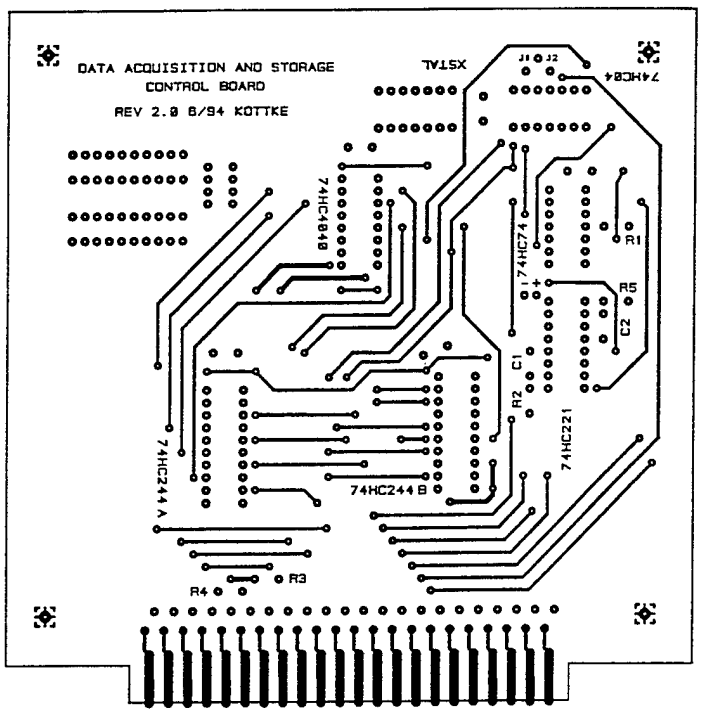

Figure 8. Artwork for the component side of the data acquisition and storage control board printed circuit board.

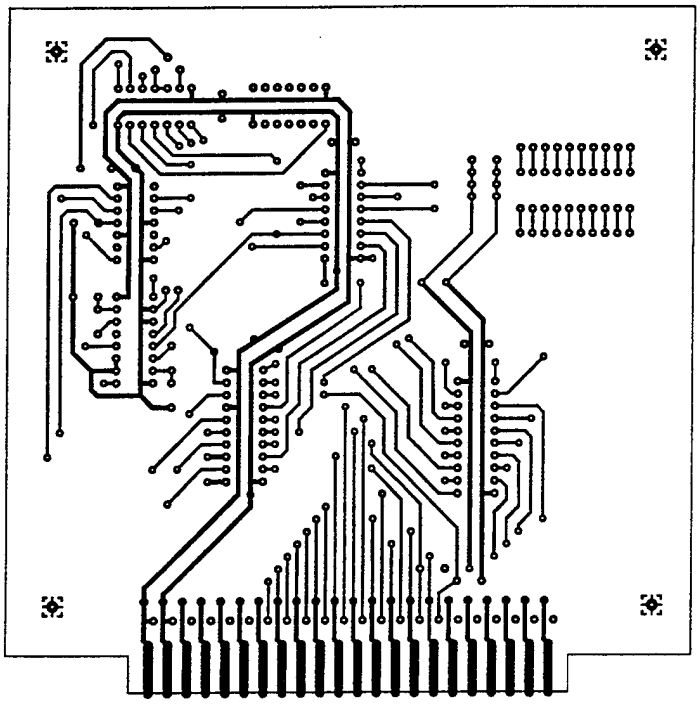

Figure 9. Artwork for the solder side of the data acquisition and storage control board printed circuit board.

Table 4. Parts List for the Data Acquisition and Storage Control Board

Description	Quantity	Part No.[a]	Cost
74HC04 hex inverter	1	MM74HC04N-ND	0.28
74HC74 dual D flip flop	1	MM74HC74AN-ND	0.38
74HC221 dual monostable multivibrator	1	MM74HC221N-ND	1.00
74HC244 octal tristate buffer	2	MM74HC244N-ND	1.36
74HC4040 12-stage binary counter	1	MM74HC4040N-ND	0.75
TTL oscillator, 4 MHz	1	X107-ND	3.38
0.1-μF ceramic capacitor	6	P4430	1.44
100-ρF capacitor	1	P4800	0.18
10-μF capacitor	1	P6343	0.22
2-kΩ resistor	1	2.00KX	0.11
4.7-kΩ resistor	3	4.75KX	0.33
100-kΩ resistor	1	100KX	0.11
DIP socket, 14 pin	3	A9414-ND	1.99
DIP socket, 16 pin	2	A9416-ND	1.50
DIP socket, 20 pin	2	A9420-ND	1.88
edgeboard connector, 44-contact, 0.156-in centers	1	S5224-ND	3.48

[a] Part numbers are as listed in Digi-Key Catalog 941. Digi-Key Corporation, P.O. Box 667, Thief River Falls, MN 56701. Tel: (800) 344-4539, FAX: (218) 681-3380.

by the pullup resistor *R1*. The momentary grounding of this line sets the *Q* output of this flip-flop high, which, in turn, is connected to the negative-edge trigger input *A bar* of the 74221 monostable multivibrator *IC4-A*. It is a subsequent drop back down to ground of the flip-flop *Q* output that will initiate the data acquisition process. Thus, the momentary grounding of the *ARM* line that pulls the *Q* flip-flop output high is what effectively arms the system. While the flip-flop output *Q* is held high, the *Q bar* output is simultaneously held low. This complementary flip-flop output can conveniently be used to drive an LED using inverted logic to visually verify the armed status. The *Q bar* signal is referred to as *ARMD* and is available on connector pin *EC2 16*.

Once the system is armed, the data acquisition process can be initiated by an appropriate transition of the *TRIG* signal on edge connector pin *EC2 30*. For flexibility, a jumper has been included to allow either positive-edge or negative-edge transitions to serve as triggering signals. A jumper in the *J1* position will configure the system for negative-edge triggering, while positive-edge triggering requires a jumper at position *J2*. With the proper jumper, the trigger signal will appear as a negative-edge transition at the reset input R_D *bar* of flip-flop *IC2-A*. This falling signal causes the flip-flop *Q* output to drop and initiate

the data acquisition process. Flip-flop output *Q bar* is simultaneously set high to extinguish the LED armed status indicator. Once the flip-flop *IC2-A* has been reset by a transition of the *TRIG* signal, additional transitions of this *TRIG* signal will have no effect on the *Q* and *Q bar* flip-flop outputs until the system is deliberately rearmed. In this way, post-triggering is eliminated.

Recall from the previous section that external control and address signals must be provided to the ADCSBs. A primary function of the DASCB is to provide these external signals. The manner in which these external signals are generated is now considered.

A negative-edge transition at the *A bar* input of the *IC4-A* monostable multivibrator initiates a number of events that begin the data acquisition process. External components *R2* and *C1* permit this monostable to generate a 300-ns positive pulse at the associated *Q* output. This positive pulse serves two functions. First, when routed to the *MR* master reset pin of the 744040 12-stage binary ripple counter *IC3*, this pulse causes the counter to clear all of its counter stages and force all of its outputs low. In other words, the positive pulse at pin *MR* resets this counter to a value of "0." The outputs from this counter are the source of the external address signals. Thus, the first address value will be 0. The second function of the positive monostable pulse is to reset a second flip-flop. After being inverted by *IC1-C*, the 300-ns pulse is directed to the R_D *bar* reset input of flip-flop *IC2-B*. As discussed, a negative-edge transition at the R_D *bar* flip-flop input forces the associated *Q* output low. The *Q* flip-flop output of *IC2-B* is routed to the *1OE bar* and *2OE bar* control lines of two 74244 tristate octal line drivers designated as *IC5* and *IC6*. The effect of a low signal on these control lines is to allow signals that are present at the input pins of these line drivers to pass through to the corresponding outputs. In effect, the low signal from the flip-flop *Q* output of *IC2-B* is used to open the electronic gates in the line drivers *IC5* and *IC6*. These open gates allow the address signals and control lines that are generated on this board to pass to the connected ADCSBs.

In addition to the positive pulse that is generated by the *Q* output, monostable *IC4-A* also generates a complementary negative pulse from its *Q bar* output. This negative pulse is used to trigger a second monostable *IC4-B* that outputs a much longer pulse approximately 1 s in duration. Such a pulse can be used to drive a piezoelectric buzzer to provide an audio confirmation of the data acquisition event.

When the 300-ns monostable pulse at the *MR* input of *IC3* terminates, this 12-bit counter is ready to begin tallying any pulses that may be present at the *CP bar* clock input. In this case, the clock pulses are

generated by the crystal oscillator *X1* and buffered by inverter *IC1-E*. The 11 least significant bits of the counter are used to produce the external address signals. The remaining most significant bit will be used to terminate the operation of this board.

Starting at the initial value of 0, each additional clock pulse increases the counter value by 1. The 11 least significant counter outputs, *Q0* through *Q10*, are routed through the enabled 74244 line drivers and are available as signals *AB0* through *AB10* on edge connector *EC2*. By connecting these signals to the system's global address bus, the storage locations of the acquired data can be controlled on the individual ADCSBs. The ADCSBs are each capable of storing 2,048 bytes of data. This data is located at addresses 0 through 2047. Thus, the data acquisition boards are full after the 744040 counter reaches a value of 2047. As this counter clocks from 2047 to 2048, the outputs *Q0* through *Q10* all take the value 0 while the most significant bit *Q11* takes the value of 1 for the first time. This positive-edge transition at output *Q11* is inverted to a negative-edge transition by *IC1-D* and routed to the S_D set input of flip-flop *IC2-B*. The low level at this set input causes the associated *Q* flip-flop output to be forced high which disables the 74244 line drivers. When disabled, the line driver outputs are placed in a high-impedance state that effectively disconnects the associated inputs from the corresponding outputs. Thus, after 2,048 storage locations are addressed, the DASCB relinquishes control of the system's global address bus.

The remaining functions of this DASCB include the generation of various control signals. During the data acquisition process, the ADCs and memory chips on the ADCSBs must be enabled for data conversion and data storage, respectively. Referring to Figure 2, the ADC is enabled for conversion by grounding control line *CE1 bar* and holding control line *CE2* high. Since *CE1 bar* is permanently grounded, the ADC is controlled by *CE2* alone through signal *ADCE*. An *ADCE* control signal is available at edge connector pin *EC2 7* as illustrated in Figure 6. When the 74244 line drivers are not enabled and their outputs are in a high-impedance state, resistor *R4* pulls *ADCE* low. Under these conditions, the ADC will be disabled if edge connectors *EC2 7* and *EC1 7* are connected. However, during the data acquisition process when the line drivers are enabled, *ADCE* is held high by the positive source voltage at the corresponding line driver input. Thus, when the line drivers on the DASCB are enabled, the ADCs on the individual data acquisition boards will also be enabled for analog-to-digital conversion.

The memory chips on the individual data acquisition boards are enabled in a similar manner. Control line *CS bar* on each SRM2016C12 RAM chip must be held low, by way of *EC1 8*, during the data storage

process. Edge connector *EC2 8* provides external control signal *MCS bar*. *MCS bar* is held high by pullup resistor *R3* when the DASCB line drivers are not enabled. However, when the 74244 line drivers are enabled during the data acquisition and storage process, *MCS bar* is held low by the ground connection at the corresponding line driver input. The *OE bar* memory chip control line is managed in a similar fashion by signal *MOE bar* at edge connector pin *EC2 9*. However, this control signal is not connected to a pullup resistor.

The only remaining control signals that need to be provided are the *R/W bar* read/write signals for the RAM chips and the *CLK* clock signals for the ADCs. Conveniently, the local clock signal on the DASCB can be used as the source for both of these control signals. Consider the timing diagram in Figure 10, which illustrates a 4-MHz clock signal across the top row. If this clock signal is provided as the *CLK* timing signal for the ADCs, then valid ADC data will be available during the time intervals displayed in the second row of Figure 10. The analog-to-digital conversion process is triggered by negative transitions of the *CLK* signal. New conversion data becomes available a maximum of 65 ns following the negative clock transition and remains valid for a minimum of 25 ns following the succeeding negative clock transition. Thus, ADC data is available during a time interval of at least 160 ns during each 4-MHz clock cycle.

In order to store the ADC conversion data, valid storage addresses must be available. These address values are generated by the 744040 counter on the DASCB, which is also clocked by the negative transitions of the 4-MHz signal. Propagation delay times for this ripple counter are 17 ns between a negative clock transition and the updating of the least significant counter bit with an additional 10 ns for the updating of each successively more significant bit. Since the 11 least significant counter bits are used for storage address generation, the maximum delay between a negative clock transition and valid counter address data will be 117 ns. As illustrated in the third row of Figure 10, this counter address data remains valid until the next negative clock transition.

The SRM2016C12 RAM chip has some timing requirements of its own. In particular, the address data that is provided to this chip must be stable for a minimum of 85 ns before any data is stored. This requirement prohibits using the positive edge of the clock pulse as a latch signal, because, at this point in time, the counter address values may be valid for less than a dozen ns. Instead, the next negative edge of the clock signal is used to store the data that was acquired by the previous negative edge. This option

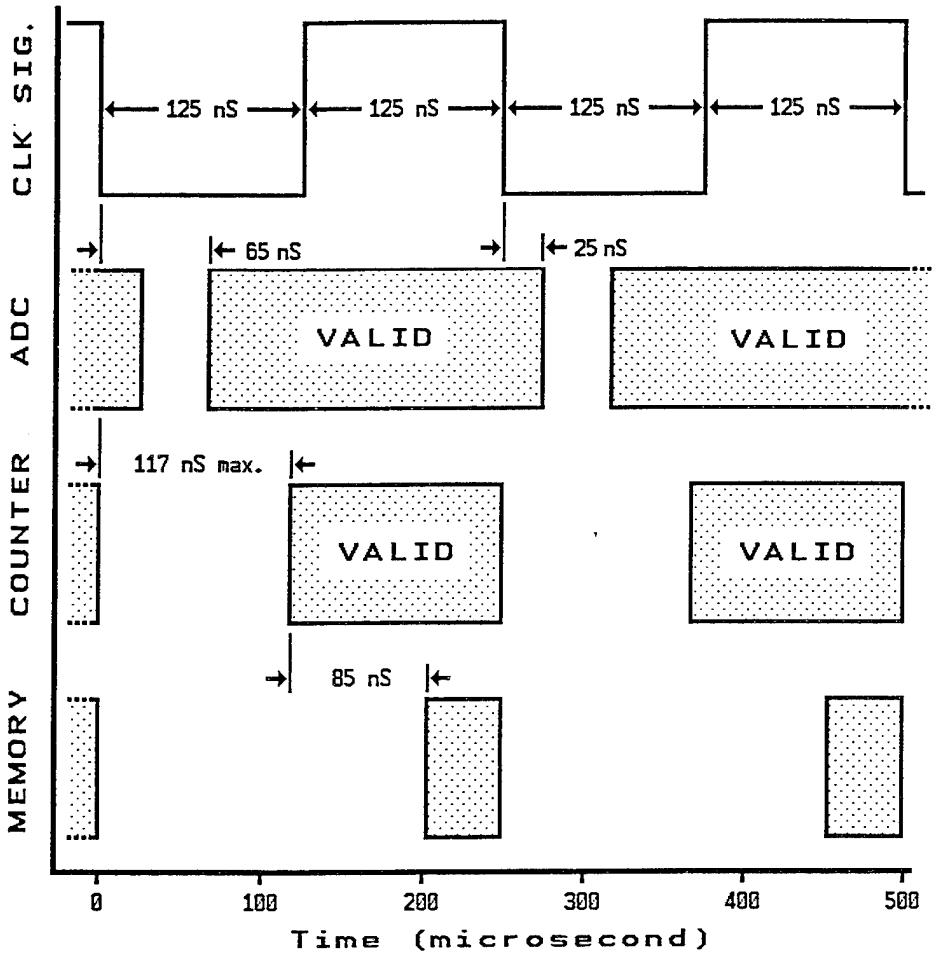

Figure 10. Timing diagram of the data acquisition and storage control board clocking signals.

is made possible by the 25-ns data hold time for the ADCs and the inherent propagation delay in the ripple counter. The only detail that needs to be dealt with is the fact that the SRM2016C12 requires a positive edge transition on the *R/W bar* line to latch data rather than the negative edge transition that the clock signal provides. This condition is easily satisfied by inverting the clock signal before using it to drive the *R/W bar* input.

2.4 Data Transfer Control Module. This module coordinates the transfer of acquired data from the individual ADCSBs to a PC for processing and long-term storage. The data is transferred along fiber optic cables that provide a high degree of electrical isolation between the site where the data is collected and the location where the experimental procedure is supervised and monitored. Such a feature is particularly desirable for tests that involve high voltages, for which operator safety is a paramount concern. A serial fiber optic communications format is employed to minimize the expense and logistics associated with this communication medium. For added flexibility, a microcontroller is used to implement the simple protocol

that allows data to be transferred in an efficient and timely manner. Figure 11 schematically illustrates the electronic circuitry that performs these operations. Once again, references to specific details on this schematic will be italicized in the following text. Table 5 enumerates the edge connector pin assignments for this printed circuit board which are also presented graphically in Figure 12. The artwork for this printed circuit board is illustrated in Figures 13 and 14. Table 6 lists the required components and their prices. The operation of this module is now presented in detail.

The DTCB is configured as a dedicated server to the PC. This hierarchy allows serial data communications to be effected using only two fiber optic cables—a control line from the PC to the DTCB and a data transfer line from the DTCB back to the PC. The PC indicates that it is ready to accept new data by transmitting a signal along the control line. Because the DTCB is a dedicated server, it can be assumed that it is capable of immediately responding to the PC's request. Therefore, an additional control line from the DTCB to the PC, to denote that data has been provided, is not required. The type of data that is to be transmitted by the DTCB to the PC along the fiber optic data link is specified by the duration of the control signal. Control signals of different durations can be used to request transmission of the next bit in the active ADCSB memory location, transmission of the first bit in the next memory location, transmission of the first bit on the next ADCSB, or a resetting of the DTCB for initiation of the data transfer process. The details of control signal timing will be reconsidered in greater depth when the microcontroller driver software is presented. For now it is sufficient to realize that the PC can request various types of data by transmitting control signals of different duration along a control line to the DTCB, which transmits the requested data bit back to the PC along a single data line.

Control signals from the PC are acquired by an HFBR-24X2 fiber optic receiver on the DTCB. This optoelectronic device incorporates an integrated photodetector and amplifier that convert light signals into equivalent electrical signals. These control signals are routed to two locations. First, they are supplied to the *RA3* input line of the 16C55 microcontroller as *PC OUT*. For testing and debugging purposes, these signals are also routed to edge connector pin *EC3 40*.

The 16C55 microcontroller is the heart of the DTCB. This device decodes the signals on the control line to determine what type of data is being requested, accesses the appropriate memory location, partitions the memory data for serial communication, and outputs this information to the PC via the data line. These microcontroller operations will now be considered in detail.

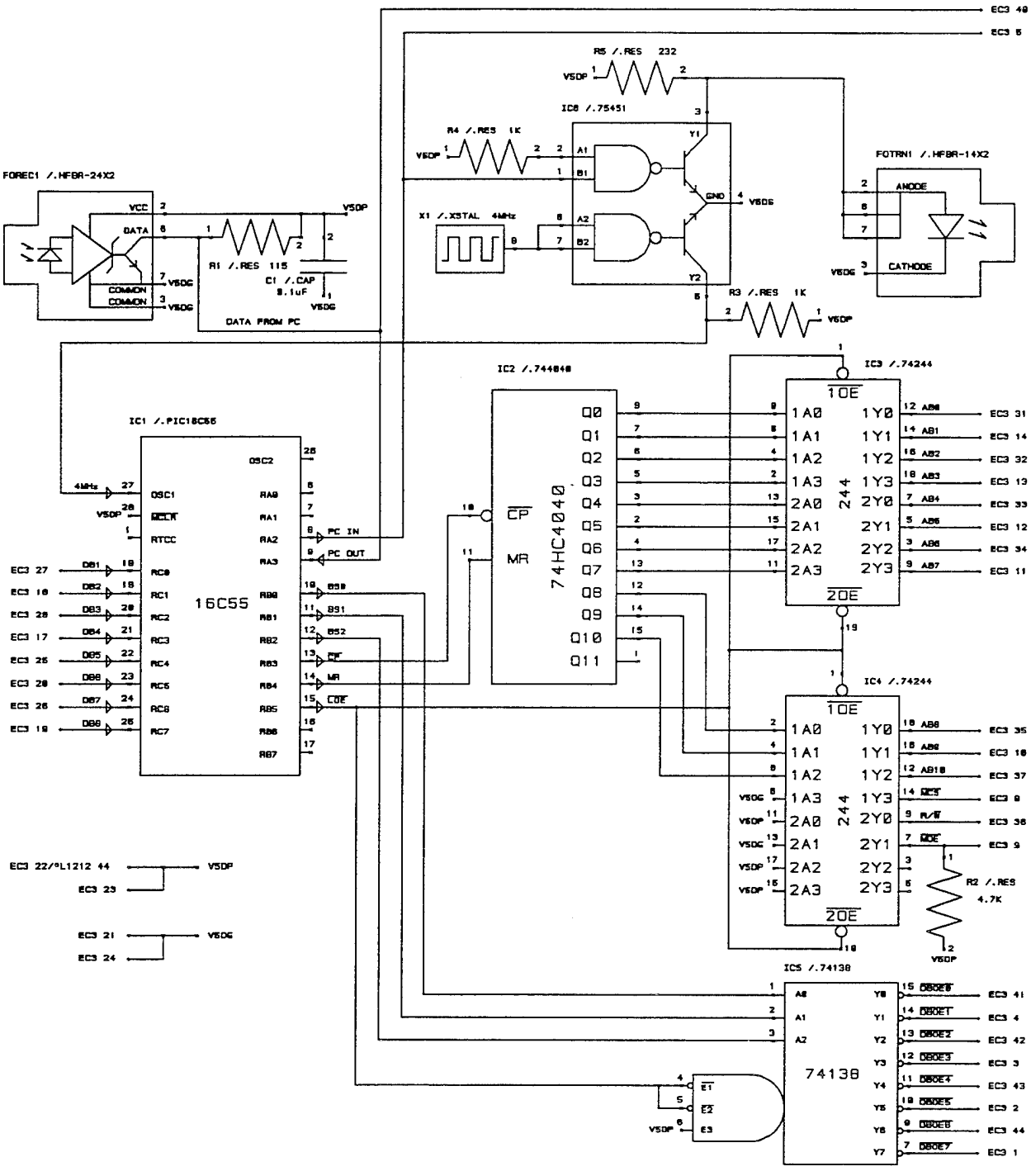

Figure 11. Electronic schematic of the data transfer control board.

Table 5. Edge Connector Pin Assignments for the Data Transfer Control Board

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	DBOE7	2	DBOE5	3	DBOE3
4	DBOE1	5	PC IN	6	none
7	none	8	MCS	9	MOE
10	AB9	11	AB7	12	AB5
13	AB3	14	AB1	15	none
16	none	17	DB4	18	DB2
19	DB8	20	DB6	21	V5DG
22	V5DP	23	V5DP	24	V5DG
25	DB5	26	DB7	27	DB1
28	DB3	29	none	30	none
31	AB0	32	AB2	33	AB4
34	AB6	35	AB8	36	R/W
37	AB10	38	none	39	none
40	PC OUT	41	DBOE0	42	DBOE2
43	DBOE4	44	DBOE6		

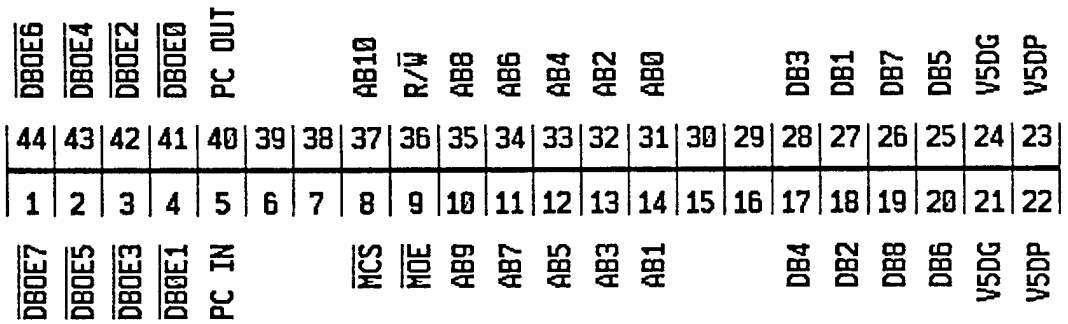

Figure 12. Edge connector pin assignments for the data transfer control board.

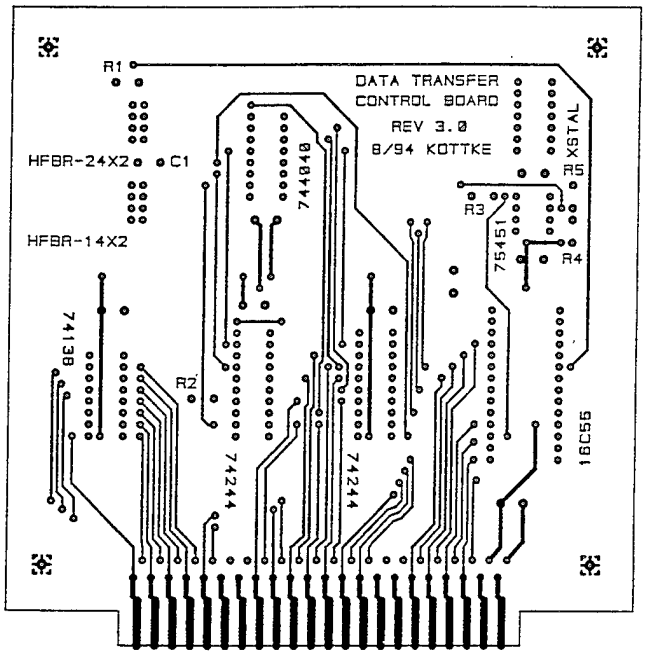

Figure 13. Artwork for the component side of the data transfer control board printed circuit board.

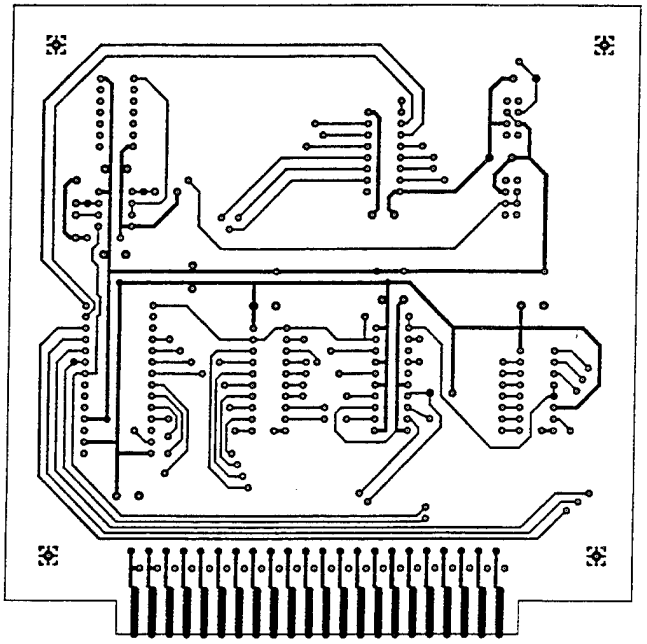

Figure 14. Artwork for the solder side of the data transfer control board printed circuit board.

Table 6. Parts List for the Data Transfer Control Board

Description	Quantity	Part No.[a]	Cost
PIC16C55 microcontroller	1	PIC16C55/JW-ND	19.13
74HC138 3- to 8-line decoder	1	MM74HC138N-ND	0.50
74HC244 octal tristate buffer	2	MM74HC244N-ND	1.36
74HC4040 12-stage binary counter	1	MM74HC4040N-ND	0.75
75451 dual peripheral driver	1	DS75451N-ND	1.33
TTL oscillator, 4 MHz	1	X107-ND	3.38
fiber optic transmitter, HFBR-1402	1	(Hewlett-Packard)	
fiber optic receiver, HFBR-2402	1	(Hewlett-Packard)	
0.1-μF ceramic capacitor	9	P4430	2.08
115-Ω resistor	1	115X	0.11
232-Ω resistor	1	232X	0.11
1-kΩ resistor	2	1.00KX	0.22
4.7-kΩ resistor	1	4.75KX	0.11
DIP socket, 8 pin	1	A9408-ND	0.40
DIP socket, 14 pin	1	A9414-ND	0.66
DIP socket, 16 pin	2	A9416-ND	1.50
DIP socket, 20 pin	2	A9420-ND	1.88
DIP socket, 28 pin	1	A9428-ND	1.32
zero insertion force socket, 28 pin	1	A303-ND	10.48
edgeboard connector, 44-contact, 0.156-in centers	1	S5224-ND	3.48

[a] Part numbers are as listed in Digi-Key Catalog 941. Digi-Key Corporation, P.O. Box 667, Thief River Falls, MN 56701. Tel: (800) 344-4539, FAX: (218) 681-3380.

As mentioned, the *PC OUT* control signals from the PC are routed to the microcontroller. Software within the 16C55 classifies the control signal by repetitively accessing a well-defined timing loop while the control signal is active. The number of executed timing loop cycles is proportional to the control signal duration. Thus, the microcontroller classifies the control signal by evaluating the magnitude of an associated timing cycle repetition counter.

Access to a particular ADCSB memory location requires that the individual board of interest be enabled and the desired memory location address be placed on the system's global address bus. The 16C55 microcontroller can enable one of eight individual boards through its three output lines *RB0*, *RB1*, and *RB2*. These three lines drive the corresponding *A#* input lines of a 74138 3- to 8-line decoder. The states of the three binary input lines determine which of the eight *DBOE# bar* output lines of the 74138 decoder will be activated. These output lines are used to enable the individual ADCSBs and give them

control of the global data bus. Data from the enabled board is transferred via this data bus to the microcontroller's *RC#* input port.

Memory addresses are generated by a 744040 12-stage binary counter. The microprocessor controls this counter through the *CP bar* clock pulse input and the *MR* master reset input, which are driven by the 16C55 output lines *RB3* and *RB4* respectively. A high signal to the *MR* input resets the counter output value to 0. Each subsequent low pulse to the *CP bar* input increases the output counter value by 1. Since the DTCB and DASCB need to share the global address bus without conflict, the counter output lines are not connected directly to this address bus. Instead, the counter outputs are buffered by a pair of 74244 octal tristate buffers that regulate the DTCB's claim to the address bus.

Once the 16C55 microcontroller has accessed a particular memory location and latched its contents through data input port *RC#*, the acquired data byte must be partitioned into individual bits for serial transmission to the PC. This operation is performed internally by the microcontroller. Through a series of masking or bit-shifting operations, the value of any bit in the data byte can be isolated and determined. These individual data bits are output as electrical signals *PC IN* through the 16C55's *RA2* output pin.

The *PC IN* data signals must be converted from electrical signals to light pulses before they can be transmitted along the fiber optic data line to the PC. This conversion is performed using a 75451 dual peripheral AND driver and an HFBR-14X2 fiber optic transmitter. The *PC IN* signal from the microcontroller is buffered by one-half of the 75451 to provide the necessary current sinking capability for control of the HFBR-14X2 transmitter. For testing and troubleshooting, the *PC IN* electrical signal is also supplied on output pin *EC3 5*. The remaining half of the 75451 is used to buffer the clock signal that paces the operation of the microcontroller.

An additional function of the microcontroller is the generation of various enabling control signals. These signals can be separated into local enabling signals, which permit various operations on the DTCB, and external enabling signals, which regulate the performance of other boards. Components on the DTCB are regulated by the local output enable signal *LOE bar*, which is generated by the microcontroller output pin *RB5*. This signal is directed to two component subassemblies. The *LOE bar* is connected to the *E1 bar* and *E2 bar* enable control inputs of the 74138 3- to 8-line decoder. When the *LOE bar* is low, a selected *DBOE#* output line from this decoder will also be low and the associated ADCSB will be

activated for data transfer. If the 74138 is not enabled by a low *LOE bar* signal, then all of its *DBOE#* output lines will be high and none of the ADCSBs will be enabled to claim the global data bus.

The *LOE bar* control line is also routed to the *#OE bar* output enable lines of the two 74244 octal tristate buffers. These buffers are used to regulate the states of the external control signals. When not enabled, the outputs of the 74244s are placed in a high-impedance state that effectively disconnects the input signals from the associated output lines. In other words, the buffer switches are "open" when these buffers are not enabled. When the *#OE bar* enable lines are pulled low by the *LOE bar*, the buffer switches are "closed" and signals are allowed to pass from the buffer inputs to the corresponding outputs. Among the signals that are allowed to pass through these buffers are the *AB#* address signals that are generated by the 744040 counter. In addition, the memory chip select *MCS bar* and memory output enable *MOE bar* lines are pulled low while the read/write *R/W bar* line is pulled high to allow the ADCSB memory chips to be enabled and to allow data to be read from them.

2.5 PC Fiber Optic Communication Module. The PC and the data acquisition hardware communicate by means of two fiber optic cables. This communication medium provides the PC environment with a high degree of electrical isolation from the data collection site. Such electrical isolation is an important safety consideration for experiments that involve high voltages. Unfortunately, the decision to employ fiber optic communications introduces the added complexity of converting between electrical signals and light signals. In other words, each fiber optic cable must have a transmitter that converts electrical signals to light signals. After passing through the cable, these light signals must be collected by a receiver that reliably converts them back to electrical signals.

These data conversion chores are handled on the data acquisition hardware end by the DTCB. Conversion on the PC end of the fiber optic cables is managed by a PC fiber optic communication board that will now be presented in detail. A simple electronic schematic of the circuitry that performs the necessary conversions is illustrated in Figure 15. Edge connector pin assignments for this board are listed in Table 7 and displayed graphically in Figure 16. Table 8 lists the components that are required to fabricate this board and their prices. An electronics board as simple as this is quite easy to hand wire. Therefore, artwork for an associated printed circuit board is not presented because the added expense would be difficult to justify against the modest potential for saving time.

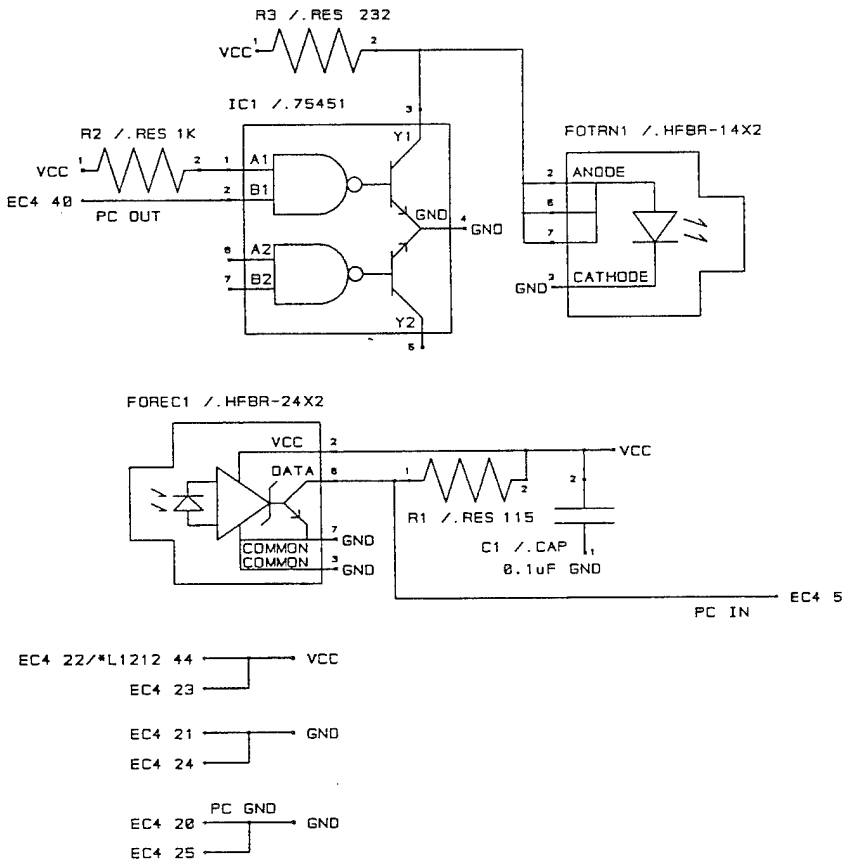

Figure 15. Electronic schematic of the PC fiber optic communication board.

Table 7. Edge Connector Pin Assignments for the PC Fiber Optic Communication Board

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	none	2	none	3	none
4	none	5	PC IN	6	none
7	none	8	none	9	none
10	none	11	none	12	none
13	none	14	none	15	none
16	none	17	none	18	none
19	none	20	PC GND	21	GND
22	VCC	23	VCC	24	GND
25	PC GND	26	none	27	none
28	none	29	none	30	none
31	none	32	none	33	none
34	none	35	none	36	none
37	none	38	none	39	none
40	PC OUT	41	none	42	none
43	none	44	none		

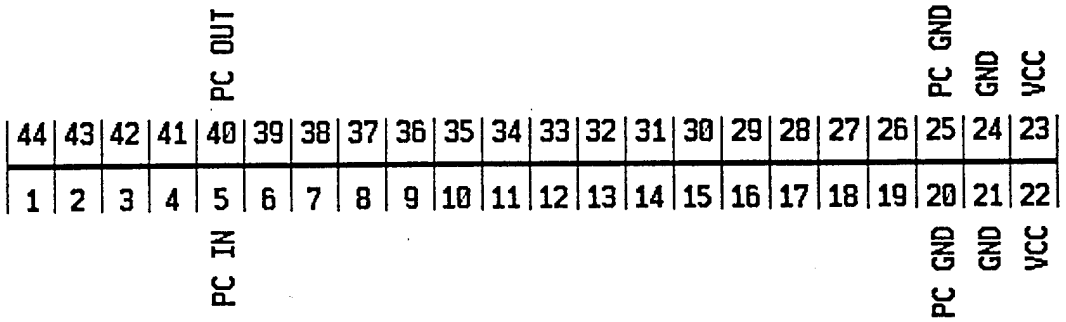

Figure 16. Edge connector pin assignments for the PC fiber optic communication board.

Table 8. Parts List for the PC Fiber Optic Communication Board

Description	Quantity	Part No.[a]	Cost
75451 dual peripheral driver	1	DS75451N-ND	1.33
fiber optic transmitter, HFBR-1402	1	(Hewlett Packard)	
fiber optic receiver, HFBR-2402	1	(Hewlett Packard)	
0.1-μF ceramic capacitor	3	P4430	0.70
115-Ω resistor	1	115X	0.11
232-Ω resistor	1	232X	0.11
1-kΩ resistor	1	1.00KX	0.11
DIP socket, 8 pin	1	A9408-ND	0.40
edgeboard connector, 44-contact, 0.156-in centers	1	S5224-ND	3.48

[a] Part numbers are as listed in Digi-Key Catalog 941. Digi-Key Corporation, P.O. Box 667, Thief River Falls, MN 56701. Tel: (800) 344-4539, FAX: (218) 681-3380.

Electrical pulses that are to be transferred from the PC to the data collection hardware are routed to edge connector pin *EC4 40* of the PCFOCB as signal *PC OUT*. These signals are buffered by one half of a 75451 dual AND peripheral driver that consists of two independent NAND gates with outputs that internally drive the bases of two uncommitted high-current, high-voltage npn transistors. The *PC OUT* signal is connected to an input of one of the NAND gates, while the other input to this gate is held high by a pullup resistor. When the *PC OUT* signal is low, the NAND gate output, and thus the connected base of the npn transistor, is held high. Under these conditions, the transistor is turned on and current flowing through the current-limiting resistor *R3* is shunted to ground through the transistor. Therefore, current does not flow through the LED in the HFBR-14X2 fiber optic transmitter and a light signal is not

output. Conversely, when *PC OUT* is high, the npn transistor is turned off which effectively disconnects the transistor from the resistor-LED series circuit. With current allowed to flow through the LED, the fiber optic transmitter outputs a light signal. Note that for this configuration the sense of the conversion is maintained during the transformation from electrical to light signals. That is, a high pulse at *PC OUT* turns the fiber optic transmitter on while grounding, or turning the *PC OUT* signal off, turns the fiber optic transmitter off.

The remainder of the circuitry on the PCFOCB converts light signals from the data acquisition hardware to electrical signals that can be input to the PC. Light signals from the data acquisition hardware are directed to an HFBR-24X2 fiber optic receiver on the PCFOCB. This device contains a photodetector and DC amplifier that drive an open collector npn output transistor. When light is incident on the photodetector, current is fed to the base of the npn output transistor which places this transistor in a conducting state. Under these conditions, the *PC IN* electrical signal at edge connector pin *EC4 5* has a low resistance path to ground through the output transistor and is therefore held low. When light is not incident on the fiber optic receiver, the low resistance path through the transistor is eliminated and the *PC IN* signal is pulled high by the pullup resistor *R1*. Note that this fiber optic receiver configuration inverts the sense of the signal during the conversion from a light pulse to an electrical signal. In other words, the presence of a light pulse forces the converted electrical signal low while the absence of an input light signal generates an electrical signal that is high.

The combination of a noninverting transmitter and an inverting receiver on a single fiber optic cable results in the inversion of all signals transmitted along this optical link. This situation can be readily accounted for in software by the drivers that control the transfer of data between the data acquisition hardware and the PC. However, it is important to keep this fact in mind when developing these drivers.

2.6 Analog-to-Digital Conversion Calibration Module. The ADCSB is equipped with a front-end amplifier that can accept and compensate for analog input signals with a wide range of magnitudes and baseline offsets. This inherent flexibility requires that the individual ADCSBs be calibrated before they can be used to record quantitatively significant information. Two methods are provided for performing this calibration. In addition to the *AINPUT* analog input, each ADCSB also has an *AOUTPUT* output that provides access to the analog signal after it has been processed by the front-end amplifier. Therefore, one calibration method is to use a dual channel oscilloscope to monitor both the input to, and output from, the ADCSB amplifier. By adjusting the amount of baseline offset and amplification, the front-end amplifier

can be calibrated to provide a desired analog output signal for a given input signal. This oscilloscope calibration method is particularly applicable when the test input signal is time variable or where determination of frequency response and inherent noise are a special concern.

A second method for calibration has been built into the ADCSB design. Each ADCSB includes a collection of buffers and LEDs that exhibit the current state of the local data bus. With the appropriate choice of control signals, the digital output of the ADC can be displayed on these LEDs. Thus, for a known DC analog input signal at *AINPUT*, the front end amplifier can be adjusted to provide the desired corresponding digital conversion value. This onboard calibration technique has the advantage of automatically compensating for the conversion response of the particular ADC. In addition, this internal calibration method obviates the need for extra calibration equipment—a handy feature when calibration must be performed in the field.

As discussed in a previous section, the ADCSB must be supplied with external control and clock signals in order to perform analog-to-digital conversions. During the usual data acquisition and storage process, these external signals are provided by the DASCB. Unfortunately, the DASCB is not a convenient generator of control and clock signals for the calibration process. The DASCB is purposefully designed to acquire just enough data to fill the memory on the ADCSB and then block further data acquisition to prevent memory overwrite. By contrast, for calibration purposes the ADC should be operating continuously so that variations in the amplifier's performance are readily displayed. The modular architecture of this data acquisition system is exploited to circumvent this apparent dilemma. During calibration, the DASCB is removed and replaced with an analog-to-digital conversion calibration board that supplies the external clock and control signals to effect continuous operation of the ADC. This very simple board will now be presented in detail. An electronic schematic of its circuitry is illustrated in Figure 17. Edge connector pin assignments are listed in Table 9 and presented graphically in Figure 18. Table 10 lists the parts that are required to fabricate this board and their prices. This board is easy enough to hand wire; therefore, printed circuit board artwork is not provided.

There are two devices on each ADCSB that can output signals to the local data bus—the SRM2016C memory chip and the CA3318C ADC. For calibration purposes, external control signals must be provided which ensure that the ADC has sole control over the local data bus. Towards this end, high signals are provided to edge connector pins *EC5 8* and *EC5 9* that provide memory chip control signals *MCS bar* and *MOE bar* respectively. Both of these signals must be held low for the memory chip to output information

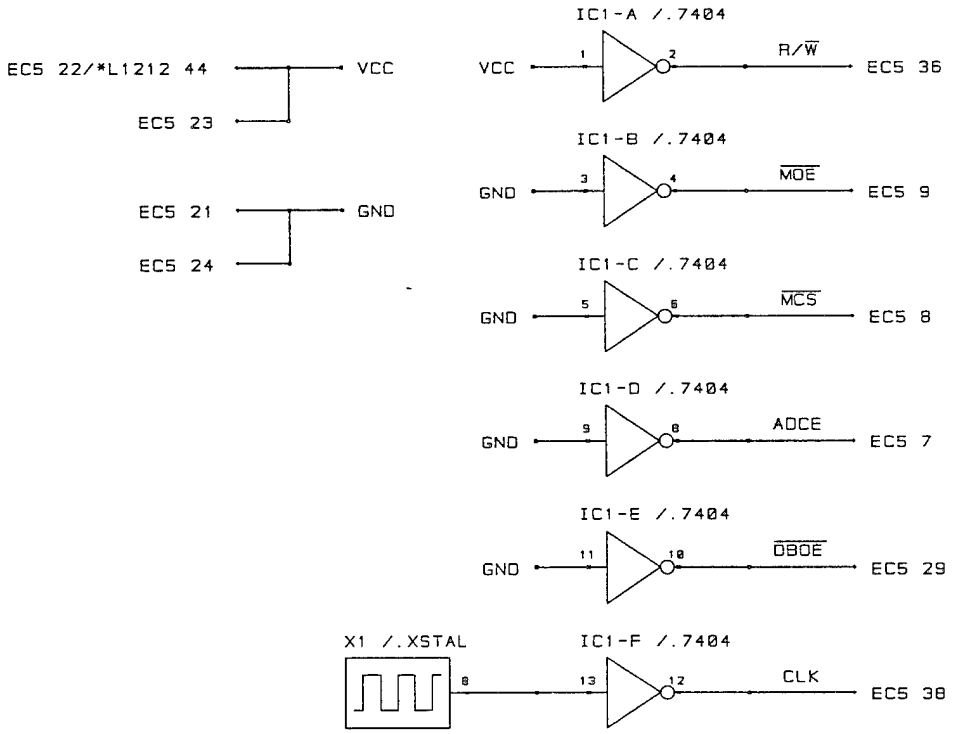

Figure 17. Electronic schematic of the analog-to-digital conversion calibration board.

Table 9. Edge Connector Pin Assignments for the Analog-to-Digital Conversion Calibration Board

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	none	2	none	3	none
4	none	5	none	6	none
7	ADCE	8	MCS	9	MOE
10	none	11	none	12	none
13	none	14	none	15	none
16	none	17	none	18	none
19	none	20	none	21	GND
22	VCC	23	VCC	24	GND
25	none	26	none	27	none
28	none	29	DBOe	30	none
31	none	32	none	33	none
34	none	35	none	36	R/W
37	none	38	CLK	39	none
40	none	41	none	42	none
43	none	44	none		

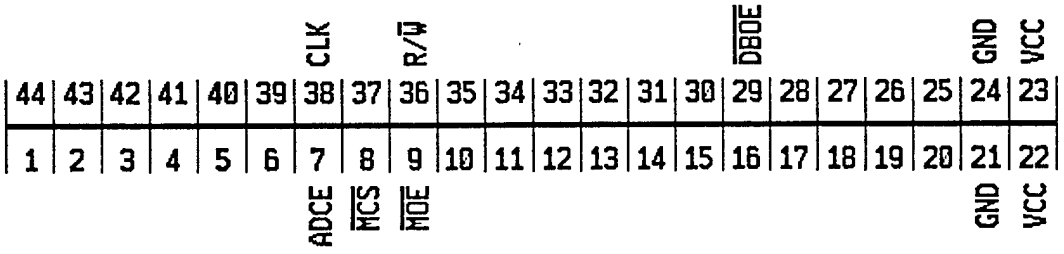

Figure 18. Edge connector pin assignments for the analog-to-digital conversion calibration board.

Table 10. Parts List for the Analog-to-Digital Conversion Calibration Board

Description	Quantity	Part No.[a]	Cost
74HC04 hex inverter	1	MM74HC04N-ND	0.28
TTL oscillator, 1 MHz	1	X101-ND	4.88
DIP socket, 14 pin	2	A9414-ND	1.32
edgeboard connector, 44-contact, 0.156-in centers	1	S5224-ND	3.48

[a] Part numbers are as listed in Digi-Key Catalog 941. Digi-Key Corporation, P.O. Box 667, Thief River Falls, MN 56701. Tel: (800) 344-4539, FAX: (218) 681-3380.

to the local data bus. Thus, by keeping these signals high, the output capability of the memory chip is disabled. In addition, the *R/W bar* memory chip control line is held low to further guarantee that the memory output lines are maintained in a high-impedance state. The ADC is enabled by providing a high *ADCE* signal to its *CE2* control pin via edge connector *EC5 7*. This combination of external control signals guarantees that the CA3318C ADC will be the only component on the ADCSB that drives the local data bus. The conversion rate of the ADC is controlled by a buffered 1-MHz clock signal *CLK* that is supplied on edge connector pin *EC5 38*.

When an ADCCB is installed in a bank of ADCSBs, all of the ADCSBs operate in parallel. That is, all the ADCSBs in that bank will process their respective analog inputs through their front end amplifiers for simultaneous analog-to-digital conversion and output on the individual onboard LED displays. By supplying the same analog input to all the ADCSBs, their relative calibration can be easily verified or adjusted. However, it is important that the signals on the individual local data buses remain on each

board. If more than one set of local data signals were to pass through to the global data bus that interconnects the individual ADCSBs, there would be considerable conflict over which ADCSB was driving this bus. This potential confrontation is avoided by providing a high *DBOE bar* signal to the data bus output driver on each ADCSB that inhibits the passage of data signals from the onboard local data bus to the global data bus. The high *DBOE bar* signal is supplied on edge connector pin *EC5 29*.

2.7 System Integration and Motherboard Design. This data acquisition system has been designed using a modular format. Each channel of data acquisition and short-term memory is contained on a separate board. In addition, the electronic circuits that control the data acquisition process and the transfer of data to long-term PC storage are also contained on their own boards. Such a compartmentalized architecture yields several advantages. System updates and conversions can be localized to the pertinent modules allowing the unaffected subcomponents to be used without modification. Field repairs can be effected by the simple removal and replacement of defective boards. Perhaps most important, the system's capacity can be tailored to the desired task by the straightforward addition or subtraction of modular data acquisition components.

Of course, the use of a modular architecture necessitates a means by which the multiple subcomponents can be integrated into a unified system. For this apparatus, the various modules are united using a communal motherboard to which the individual boards are attached. The design and operation of this motherboard will now be presented in detail. An abbreviated electronic schematic of the motherboard wiring is presented in Figure 19, while scaled versions of the printed circuit board artwork are illustrated in Figures 20 and 21. The motherboard terminal strip pin assignments are enumerated in Table 11 and displayed graphically in Figure 22.

The data acquisition and data transfer control modules are each designed to interface with a maximum of eight data acquisition and storage boards. Therefore, the motherboard has been designed to accommodate one DASCB, eight ADCSBs, and one DTCB. During calibration procedures, an ADCCB can be substituted for the DASCB. The previously described PCFOCB must be located with the PC that is used for long-term data storage and therefore is not associated with this motherboard. An 8.5- x 11-in schematic of the motherboard that displays all the connections between the 10 control and acquisition boards is illegible at best. Therefore, Figure 19 illustrates an abbreviated schematic of the motherboard that includes one DASCB, only two ADCSBs, and one DTCB. Little information is lost

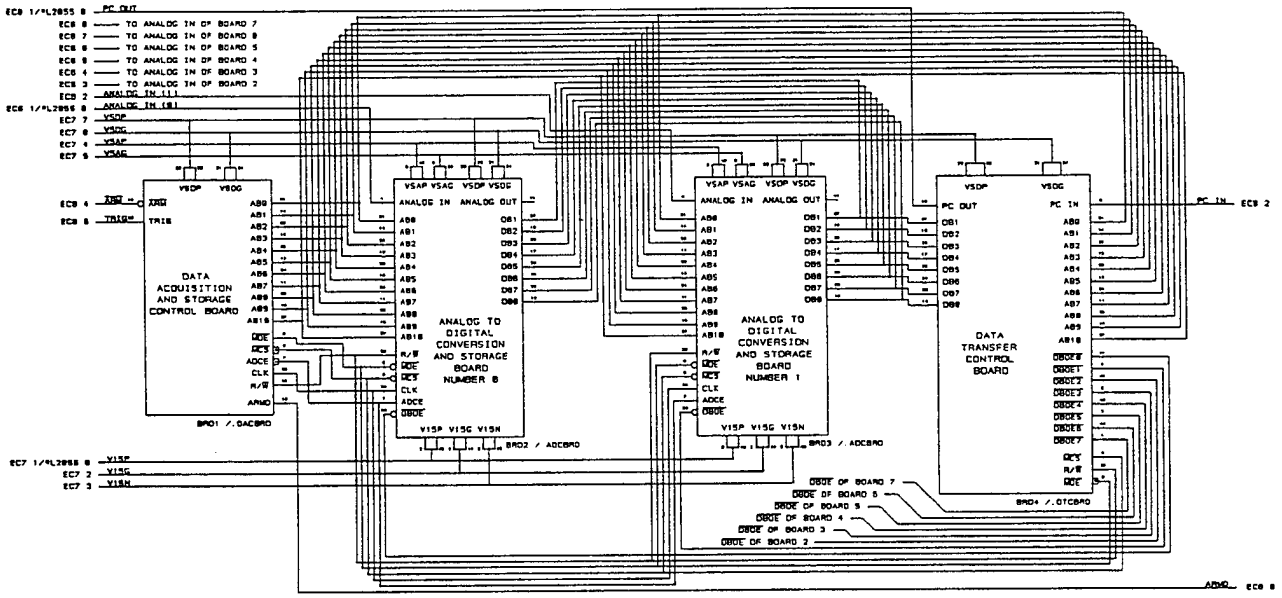

Figure 19. Abbreviated electronic schematic of the motherboard.

using this condensed schematic, because the connections to the eight ADCSBs are all similar and pertinent connections to the boards that are not illustrated are described in the schematic by text.

The main connections between the various modules via the motherboard include the power lines, the address bus, the global data bus, and a collection of control signals. Power is provided to the ADCSBs for onboard analog signal processing through *V15P*, *V15N*, *V15G*, *V5AP*, and *V5AG*, which are accessed through terminal strip pins *EC7 1*, *EC7 3*, *EC7 2*, *EC7 4*, and *EC7 5* respectively. *V15P* and *V15N* are +15- and -15-V power lines referenced to the *V15G* ground while *V5AP* is a +5-V power line referenced to the *V5AG* ground. All of the modules are provided with the +5-V digital power line *V5DP* that is referenced to the *V5DG* ground. The digital power line and its ground are accessed by terminal strip pins *EC7 7* and *EC7 8* respectively. Separate +5-V power lines are provided for the analog and digital components in an effort to isolate the analog circuitry from the switching noise that is common on digital power networks. LED indicators on the motherboard show when these power lines are activated.

The motherboard address bus allows the data acquisition and data transfer control modules to access specific short-term memory locations on the ADCSBs. Information is transferred between the controllers

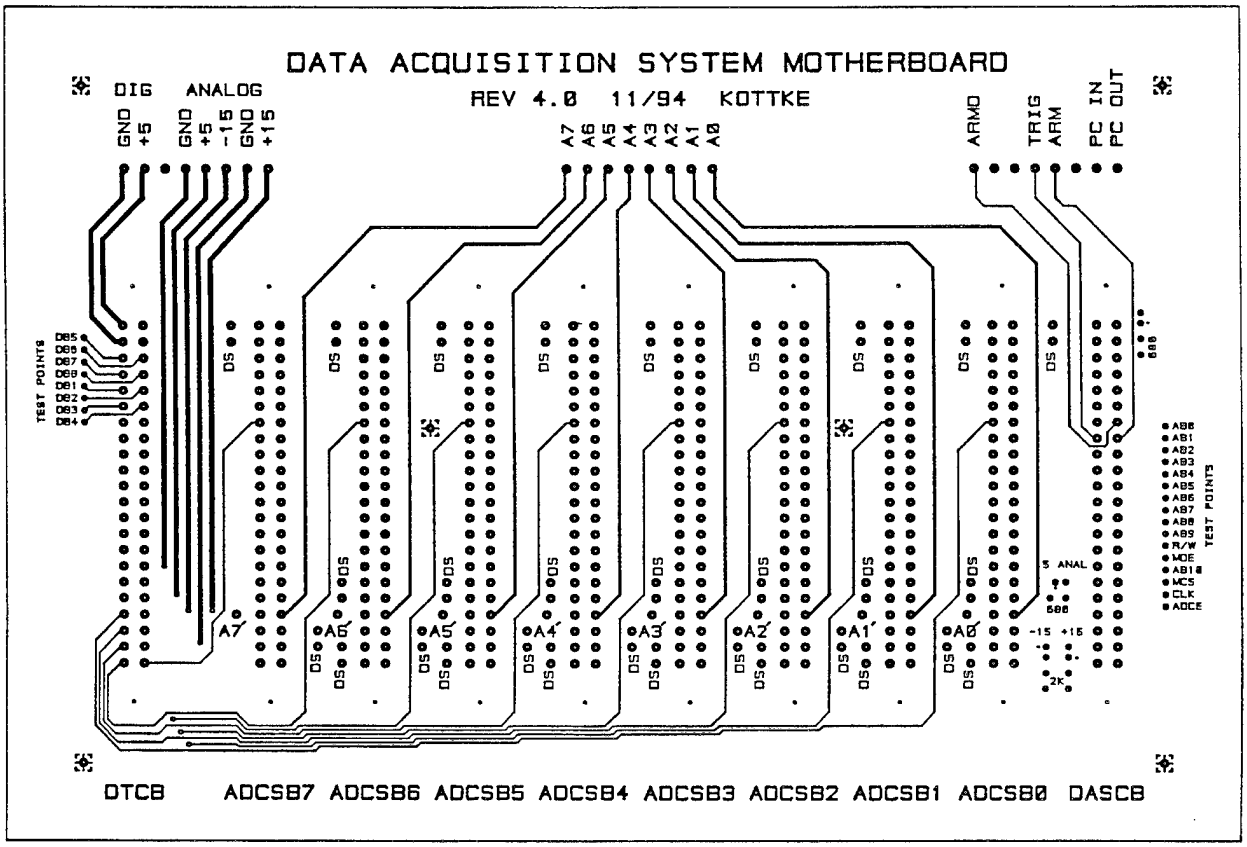

Figure 20. Artwork for the component side of the motherboard.

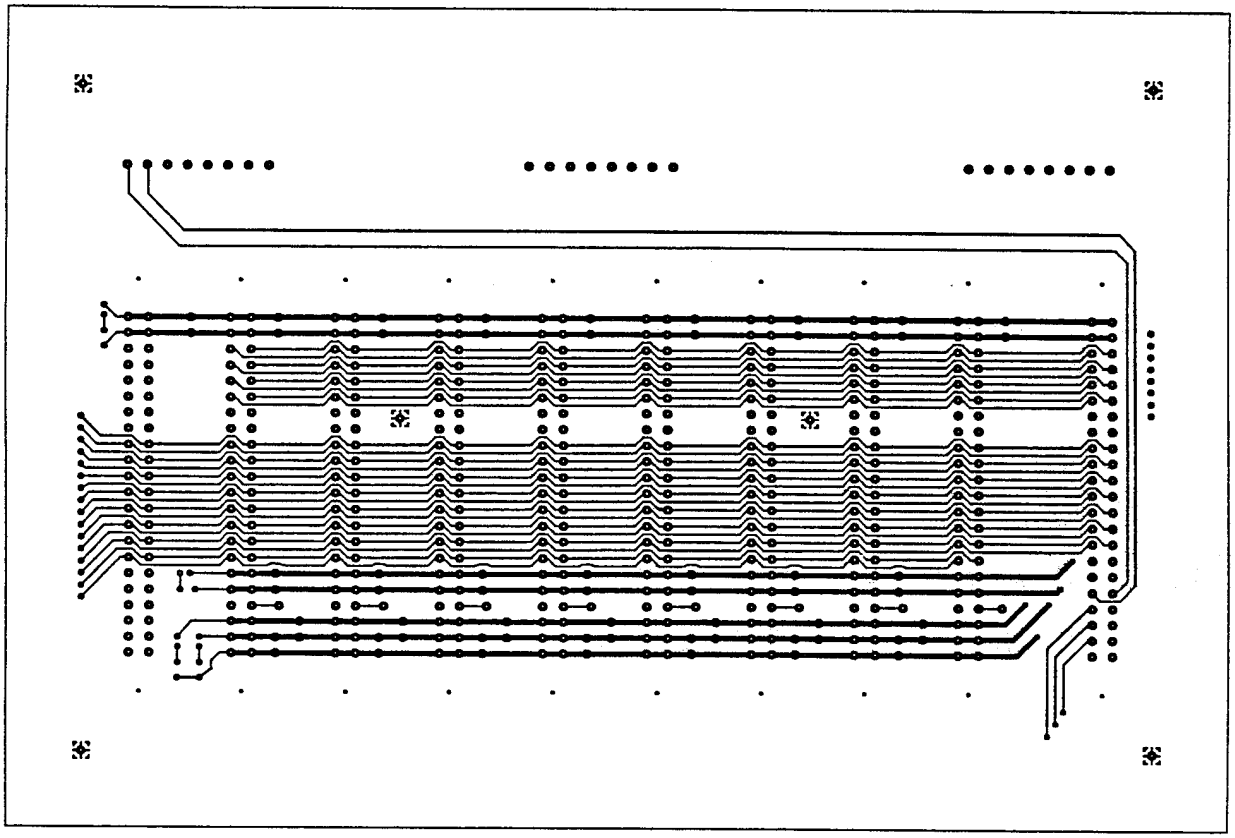

Figure 21. Artwork for the solder side of the motherboard.

Table 11. Terminal Strip Pin Assignments for the Motherboard

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
EC6 1	ANALOG IN 0	EC7 1	V15P	EC8 1	PC OUT
EC6 2	ANALOG IN 1	EC7 2	V15G	EC8 2	PC IN
EC6 3	ANALOG IN 2	EC7 3	V15N	EC8 3	none
EC6 4	ANALOG IN 3	EC7 4	V5AP	EC8 4	ARM
EC6 5	ANALOG IN 4	EC7 5	V5AG	EC8 5	TRIG
EC6 6	ANALOG IN 5	EC7 6	none	EC8 6	none
EC6 7	ANALOG IN 6	EC7 7	V5DP	EC8 7	none
EC6 8	ANALOG IN 7	EC7 8	V5DG	EC8 8	ARMD

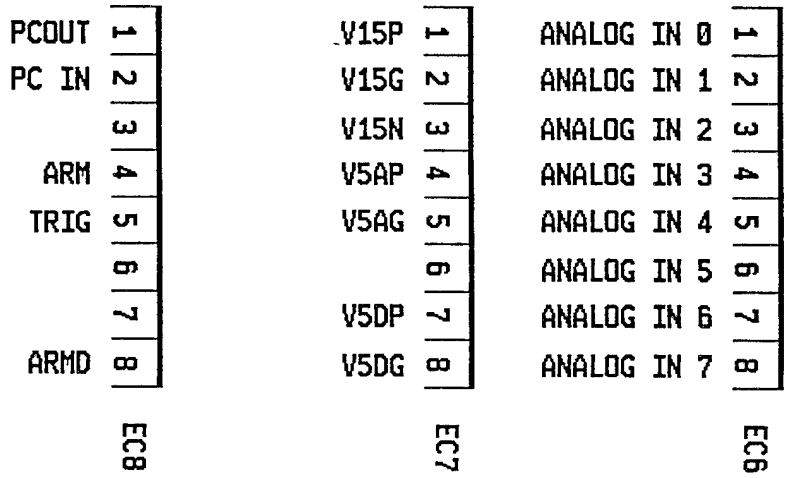

Figure 22. Terminal strip pin assignments for the motherboard.

and the ADCSBs by way of the global data bus. Both of these buses are internal to the motherboard and thus access is not provided to their signals via terminal strip connectors. However, to facilitate troubleshooting operations, access to these signals, and a variety of other control signals, is provided through a series of test points labeled *AB#* and *DB#* as illustrated in Figure 20.

The only difference between the motherboard connections to the individual ADCSBs is the provision for a separate *ANALOG IN* external input to each board and a unique *DBOE bar* line between each ADCSB and the DTCB. External analog input signals *A0* through *A7* are supplied via terminal strip *EC6*. Note that a test point *A# prime* is provided for each analog signal after it has been processed by the amplifier on its ADCSB. The various *DBOE bar* control signals are provided by the DTCB and allow each

ADCSB to take control of the global data bus during data transfer to the PC. Finally, terminal strip *EC8* provides access to the arming, triggering, and PC data transfer signals.

3. DATA ACQUISITION SYSTEM SOFTWARE

3.1 Software Overview. A collection of ADCSBs and a DASCB are used during the data acquisition process. The logic on these boards is totally hardwired and therefore no software is required for their operation. However, the subsequent transfer of acquired data from the short-term memory of the ADCSBs to the long-term storage of a PC hard drive is orchestrated by a DTCB. This board includes a PIC16C55 microcontroller that requires a driver program for its operation. The PC to which the data is transferred also needs a suitable driver program. Thus, the data transfer process requires appropriate software for both the DTCB microcontroller and the PC. Software control of the data transfer process provides a flexible format that can be readily adjusted to accommodate future upgrades and system reconfiguration. This software is now presented in detail.

3.2 PC Driver Software. Data is transferred from the ADCSBs to the PC for long-term storage on a hard drive. During the transfer process, the PC operates as a master device that instructs the servant PIC16C55 microcontroller when and what type of data to provide. This hierarchical arrangement allows data to be transferred using only two serial lines—a control line from the PC to the microcontroller and a data line from the microcontroller back to the PC. Thus, the essential functions of the PC driver software involve the generation of appropriate microcontroller control signals and the reading of data sent from the microcontroller.

Of course, in reality, the PC driver software performs many more functions as illustrated by the flowchart in Figure 23. A listing of the PC driver software is provided in Appendix A. This code was developed in the Microsoft* QuickBasic 4.5 programming environment. This program starts off by defining a number of variables that determine the I/O card base address, the duration of required time intervals, and graphic display colors. Due to the serial nature of the transfer process, the data is transmitted one bit at a time. Thus, after transmission, each data byte must be reconstructed from its constituent data bits. During this reconstruction, each data bit must be multiplied by an appropriate power of two and summed with the other bits in the data byte. To save processing time, these powers of two

* Microsoft is a registered trademark of Microsoft Corporation.

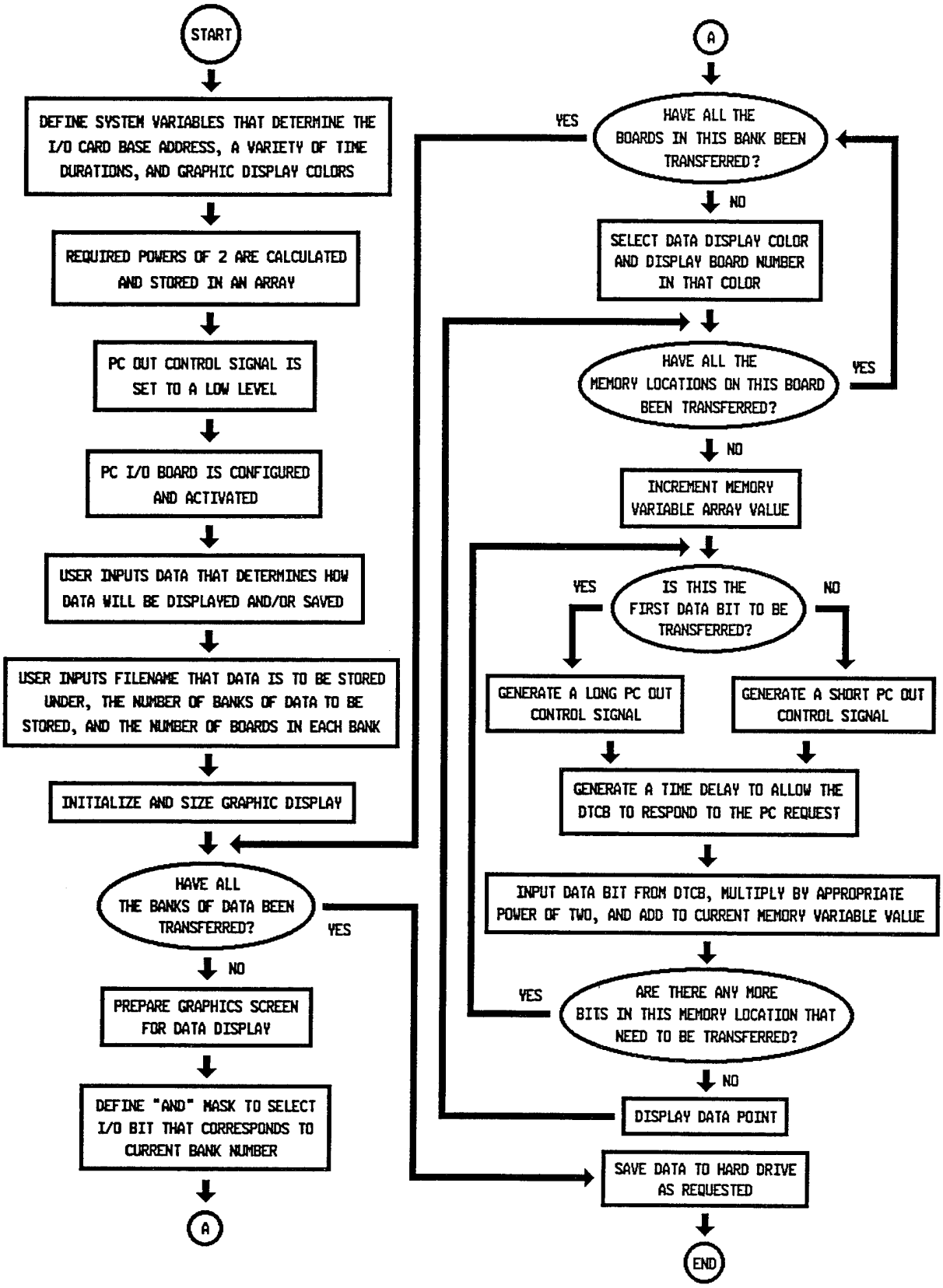

Figure 23. Flowchart of the PC driver software.

are calculated in advance, stored, and retrieved as necessary. The *PC OUT* control signal is then set to an initial low state.

A National Instruments PC-DIO-24 digital input/output card was used to get the control signals out of, and the data signals into, the PC. It is this card that required the earlier base address definition. This I/O card includes three different 8-bit ports that can operate in a number of modes. Therefore, this card must be properly configured before it is used. The PC driver program accesses a subroutine that performs this configuration and activates the card for digital input and output. The details of the configuration process are covered in the PC-DIO-24 User Manual.*

At this point, the PC driver software queries the user about the manner in which the transferred data is to be displayed, whether the data is to be saved on hard disk, and the configuration of the data acquisition system. As many as eight ADCSBs can be controlled by a single DASCB. Each DASCB and the associated ADCSBs is referred to as a "bank." The user must input the number of banks, the number of ADCSBs associated with each bank, and a data file name prefix that will identify files stored on the hard disk. Stored data files are uniquely labeled by concatenating the data file prefix with the bank number and board number. The PC driver program then prepares the graphic screen for data display and initiates the data transfer process.

The PC is capable of making two requests of the DTCB via the control line. These two requests can be paraphrased as:

1) "Give me the first bit of data."
2) "Give me the next bit of data."

Control signals are classified by their duration. A request for the first data bit consists of a high control signal with a long duration, while control signals for the next data bit are high signals with a much shorter duration. When the DTCB of any bank is asked to send the first data bit, it will always transmit the least significant bit of the lowest memory location of ADCSB number zero. The reaction of a DTCB to a PC request for the next data bit depends on the current status of the data transfer process. If a memory location has been partially transmitted, then a PC request for the next data bit will cause the DTCB to

* National Instruments Corporation. PC-DIO-24 User Manual. 1990.

transfer the next most significant bit of the ADCSB memory location that has been partially transferred. After all the bits from a given ADCSB memory location have been transferred, a subsequent PC request for the next data bit will cause the DTCB to transfer the least significant bit of the next ADCSB memory location. When all the bits of all the memory locations on a given ADCSB have been transferred, the succeeding PC request for the next data bit will instruct the DTCB to transfer the least significant bit of the lowest memory location on the next ADCSB. When all the data has been transferred from all the boards associated with a given bank, the data on the next bank is treated in a similar fashion. A short time delay is included between the generation of all PC control signals and the subsequent reading of data by the PC. This delay allows the DTCB sufficient time to provide the requested data. Finally, the transferred data is displayed on the PC monitor and saved on the PC hard drive as requested by the operator.

3.3 Microcontroller Driver Software. A PIC16C55 microcontroller on the DTCB monitors the control line for instructions from the PC and manages the transfer of requested data from the ADCSBs to the PC via the data line. The microcontroller software that performs these functions is listed in Appendix B and displayed graphically in flowchart format in Figure 24. This code has been written for assembly by the Microchip* Technology MPALC macro assembler. The macro capability of this assembler has been extensively used to produce a highly modular and flexible code. Macro names are denoted in the flowchart of Figure 24 by square brackets. Following assembly, this code is downloaded into the PIC16C55's EPROM where it is automatically executed after the system is powered up.

The PIC16C55 microcontroller includes 21 I/O data lines that default to an input configuration on power up. For this application, the microcontroller must perform data output operations as well as data input. Therefore, the PIC16C55 I/O port directions are configured as required by the macro *SetTRIS*. The PIC16C55 also contains a free running on-chip RC oscillator that can function as a watchdog timer to place the microcontroller in a low-power sleep mode if it remains inactive for an extended period of time. This option is not used for this application. To avoid unnecessary watchdog intervention, the macro *SetOPTION* is executed to maximize the time interval between watchdog timeouts.

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* Microchip and MPALC are registered trademarks of Microchip Technology Inc., 2355 W. Chandler Blvd., Chandler, AZ 85224-6199. Tel: (602) 786-7200.

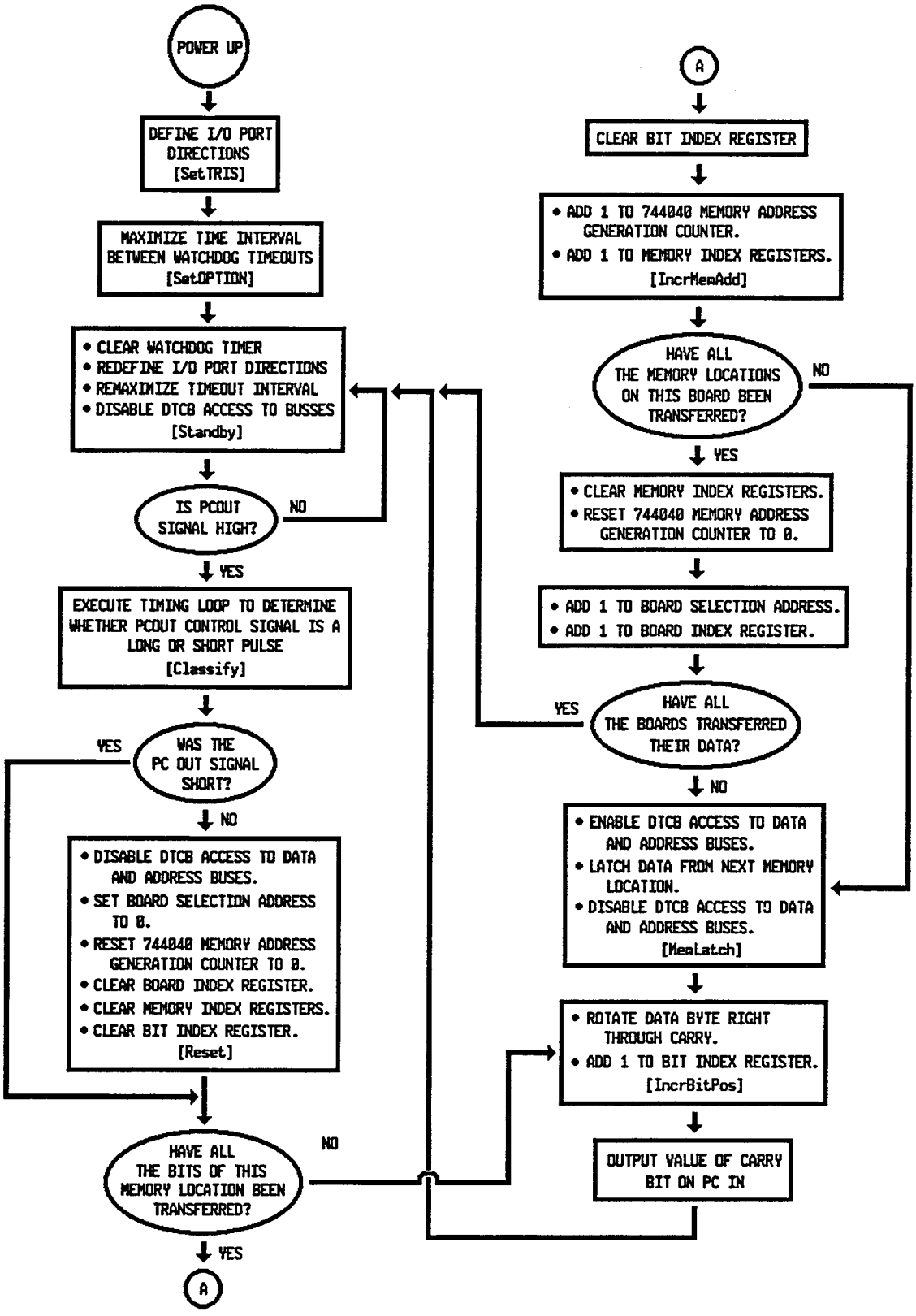

Figure 24. Flowchart of the data transfer control board microcontroller driver software.

When executed, the macro *Standby* places the microcontroller in an inactive but alert status. This macro is used as a return location for many of the code's operations. Specifically, this macro clears the watchdog timer, redefines the I/O port directions, remaximizes the timeout interval, and disables the DTCB's access to the address bus. The watchdog timer is cleared to avoid the previously mentioned sleep mode. Operation in electronically noisy environments can result in corruption of the contents of the microcontroller's registers. Thus, the manufacturer recommends[4] that all I/O control registers be redefined at regular intervals. It is for this reason that the *Standby* macro redefines the I/O port directions, remaximizes the timeout interval, and redisables the DTCB's access to the address bus. In this way, potential conflicts between the DTCB and the DASCB are avoided.

At this point, the microcontroller enters a loop that monitors the control line for possible PC data requests. As long as the *PCOUT* signal remains low, the microcontroller simply reconfirms its standby status before once again checking the state of this control line. A high *PCOUT* signal indicates that the PC is making a data request. As previously discussed, the PC can make two types of data requests that are differentiated by the duration of the *PCOUT* control signal. The control signal is categorized by the macro *Classify*. This macro repeatedly exercises a loop that increments the value of an 8-bit register and checks to determine whether the register has "rolled over" to a value of zero. Long control pulses will allow this counting register to be incremented a sufficient number of times to be rolled over. Conversely, short control pulses will not provide the counting register with the necessary time to roll over. Thus, it is the effective carry status of this counter register that is used to classify the *PCOUT* control signals.

A long control signal is used to denote a request for the first bit of data from a particular bank of ADCSBs. By definition, this first data bit is the least significant bit of the lowest memory location of the number zero ADCSB. The PIC16C55 microcontroller prepares for the transmission of this first data bit by taking the following actions:

1) The 74HC138 3- to 8-line decoder, that is used to select the enabled ADCSB, is configured to access ADCSB number 0. The board index register on the 16C55 that tracks the active ADCSB is also cleared to zero.

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[4] Microchip Technology Inc. Microchip Data Book. Chandler, AZ, Second Edition, 1992.

2) The 74HC4040 12-stage binary ripple counter, that is used to generate the current ADCSB memory address, is reset to 0 along with the 16C55 memory index registers that tracks this value.

3) The 16C55 register that is used to track the current bit location within the active memory location is reset to 0.

These actions guarantee that the transmitted data bit will be the first bit on the active bank.

A control signal of a short duration is interpreted as a request for the "next" data bit. As discussed, the response to this request depends on the current status of the transmission process. If the current memory location has been only partially transmitted, then the bit index register will be incremented and the next most significant bit in the current memory location will be transferred. If the previous transition transferred the most significant bit of a memory location, then, if there are more significant memory locations on the active ADCSB, a request for the next data bit will increment the memory index register, reset the bit index register to zero, and transfer the least significant bit of the next most significant memory location. If all the data from a given ADCSB has been transferred, then the board index register will be incremented, the memory index and bit index registers will be cleared, and the first bit of the next most significant board will be transferred. This process continues until all the data associated with a bank has been transferred to the PC.

4. DATA ACQUISITION AND TRANSFER SYSTEM EVALUATION

4.1 Data Acquisition Performance. This data acquisition system has been designed to record bipolar signals with amplitudes in the range from several to 100 V and frequencies on the order of several kilohertz with a sampling rate of up to 4 MHz. The CA3318C 8-bit flash analog-to-digital converters used in this system are capable of quantifying only unipolar signals with a full-scale, input-voltage range of 4 to 7.5 V. Thus, these A/D converters require additional signal processing circuitry to scale the input signal to the acceptable measurement range. The performance of this signal processing circuitry, the A/D converters, and the short-term storage memory is quantified by feeding a well-characterized signal to the data acquisition system and evaluating the recorded information.

Figure 25 illustrates the data that the system recorded for a 10-kHz bipolar sine wave with a peak-to-peak amplitude of 10 V. Prior to measuring this input signal, the amplification factor and baseline of the

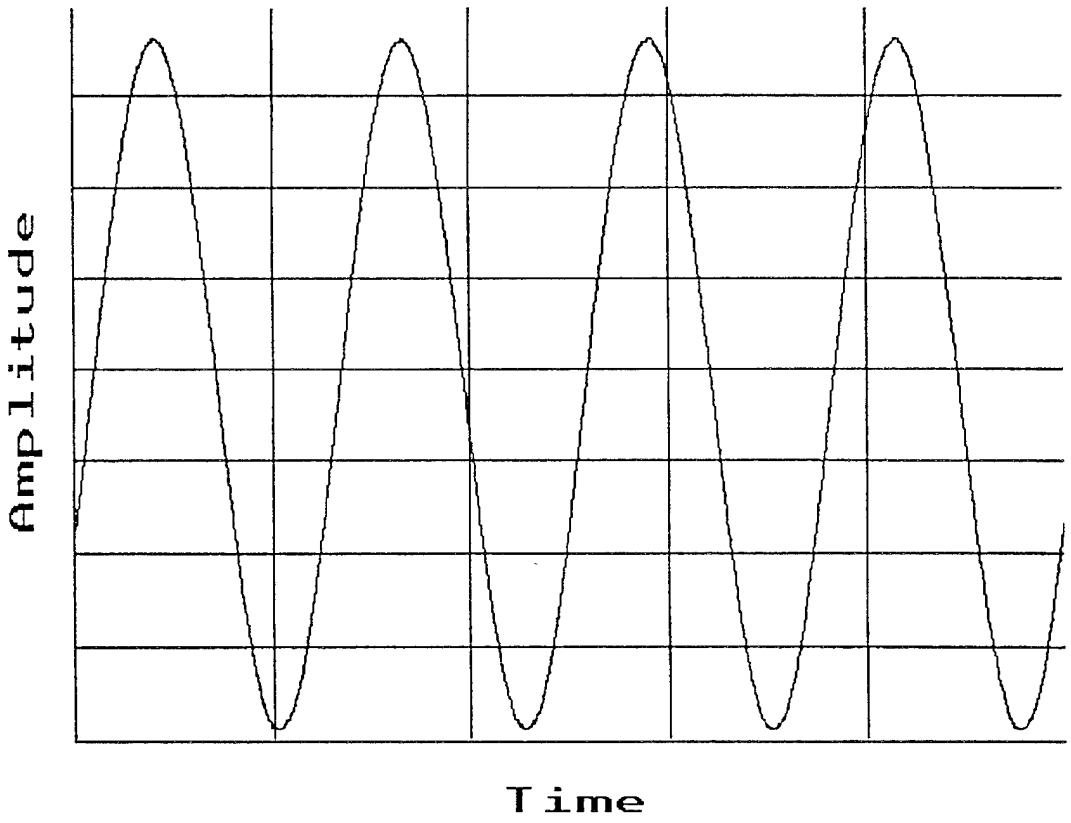

Figure 25. Illustration of 10-kHz sine wave recorded by data acquisition system.

signal processing preamplifier were adjusted to accept input signals over the range from -5 to +5 V. An enhanced data sampling rate of 5 MHz was used for these measurements that corresponds to 0.2 μs per sample. The horizontal span between the vertical grid lines represents 400 data points. Thus, the five horizontal intervals that are displayed in Figure 25 represent a total of 2,000 samples or a measurement time spanning 400 μs. A 10-kHz signal has a period of 100 μs. Therefore, during a 400-μs measurement interval, the data acquisition system should record four complete cycles of the 10-kHz input signal. The fact that Figure 25 does indeed reveal four such cycles demonstrates that the data acquisition system is capable of sampling data at the required rate. This figure also indicates that the inherent noise associated with the measurement system is on the order of the ADC's resolution.

The data acquisition system's frequency response is investigated by increasing the frequency of the input signal to 100 kHz. Figure 26 illustrates the data that was recorded for this input signal using the same sampling parameters described in the previous paragraph. Note that the recorded amplitude of the 100-kHz signal is very nearly the same as that of the 10-kHz signal. This indicates that at 100-kHz the signal processing preamplifier is experiencing very little high-frequency "roll off." Thus, the frequency

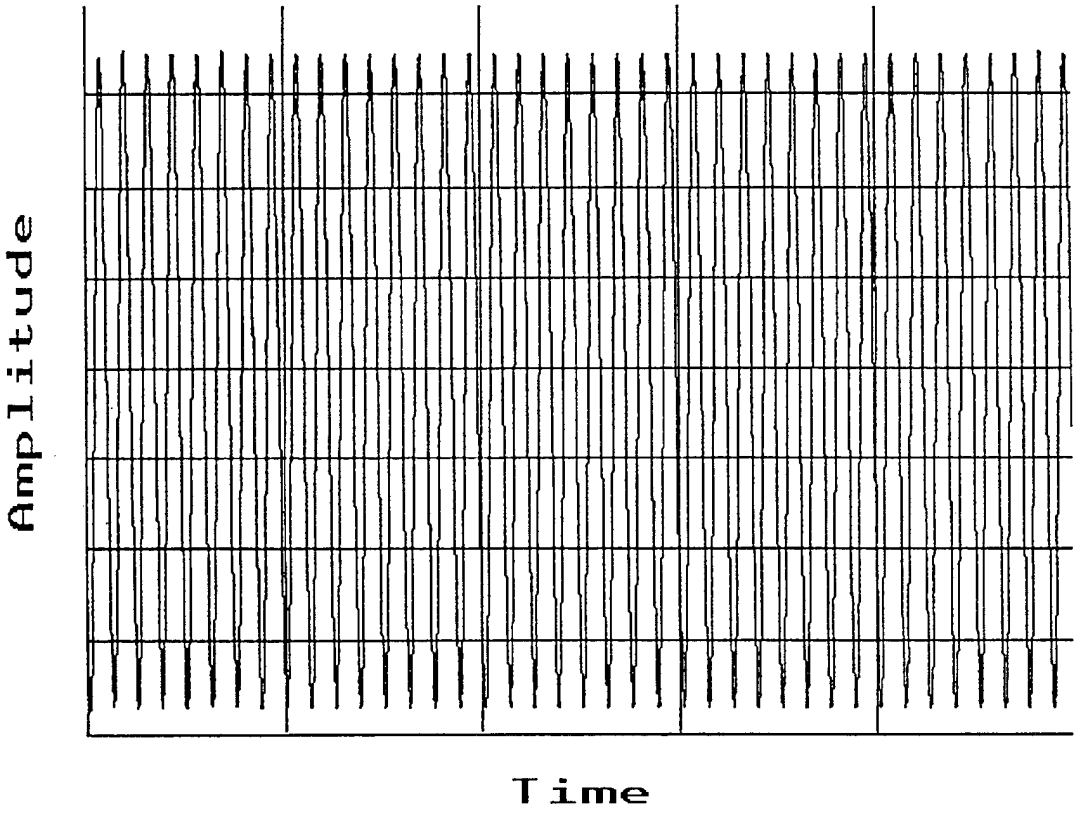

Figure 26. Illustration of 100-kHz sine wave recorded by data acquisition system.

response of the data acquisition system is concluded to be sufficient to accurately record input signals with frequencies of several tens of kilohertz.

4.2 Data Transfer Performance. As each data value is measured by a CA3318C ADC, it is saved in an SRM2016C12 static RAM chip. These memory devices are static to the extent that their contents do not need to be periodically updated or refreshed. However, once these memory chips are powered down, the information that they contain is lost. It is for this reason that the contents of these short-term memory components need to be transferred to a long-term storage device such as the hard drive on a PC.

In an era when more powerful and faster computers become commercially available on a monthly basis, computer users are becoming increasingly intolerant of lengthy access times. For this reason, the process that transfers data from the short-term memory of the ADCSBs to the long-term storage of a PC hard drive has been optimized to tax the users patience and attention span to a minimal degree. In addition to simply writing efficient software to drive the data transfer process, the time delays incorporated into these drivers to allow sufficient time for the various transfer processes have been made variable. By

successive trial-and-error testing, these time delays can be pared down to the minimum values that will allow data to be transferred in an accurate and efficient manner. Data transfer rates were also increased by boosting the clock speed of the 16C55 microcontroller on the DTCB up to 10 MHz and running a compiled rather than an interpreted version of the PC driver software. The performance of the data transfer process was evaluated using a less than cutting edge PC with an 80286 microprocessor clocking at 12 MHz. For this system, all the data can be transferred from one bank containing eight ADCSBs and displayed as a collection of data points on the PC monitor in less than 12 s. To transfer the data, display it, and save it on the PC hard drive requires 25 s.

5. SUMMARY

A data acquisition system is presented that allows multiple channels of information to be captured and stored at high rates. Although designed to satisfy a specific need, this apparatus is flexible enough to adapt to a wide range of data logging requirements. The source of this flexibility is a modular architecture that allows the data collection capability to be tailored to specific scenarios by the straightforward addition or subtraction of standardized components. Each signal that is to be monitored is routed to a separate analog-to-digital conversion and storage board. These conversion and storage modules adjust the magnitude and baseline of the input analog signals, perform high-speed analog-to-digital conversions, and store the conversion values in short-term random access memory. Each channel can acquire and record 2,048 data points of 8-bit data at sampling rates up to 5 MHz.

The actions of the individual conversion and storage boards are coordinated by a centralized data acquisition and storage control module. A single data acquisition control module can arm and trigger the acquisition process and provides the control and address signals to oversee up to eight channels of data input. Following the data acquisition process, a data transfer control module is used to orchestrate the transfer of the recorded information from the short-term random access memory of the individual analog-to-digital conversion and storage boards to the hard drive of a PC for processing and long-term storage. Data is transferred along fiber optic cables to provide a high degree of electrical isolation between the site where the data is collected and the location where the experimental procedure is supervised and monitored. The application of fiber optic data links necessitates the use of a PC fiber optic communication module that converts between electrical and light signals. This module can be omitted if fiber optic links are not employed.

The final module to be presented is an analog-to-digital conversion calibration board. Substitution of this module for the data acquisition and storage control board allows the signal processing amplifiers on each data acquisition and storage board to be readily calibrated using onboard data display capabilities.

The integration of this multitude of modules into a unified system is expedited by the use of a communal motherboard, to which the individual boards are attached. This motherboard provides the power, address bus, global data bus, and control signals connections that are required between the various printed circuit boards. In addition, this motherboard supplies the user with convenient access to all pertinent signals.

This report provides all the technical information that is required to maintain, expand, or even duplicate this apparatus. Towards this end, schematic diagrams, operational descriptions, printed circuit board masks, and parts lists are provided for all the major module types. In addition to these hardware considerations, examples of required software drivers are also presented and interpreted.

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APPENDIX A:

PC DRIVER SOFTWARE FOR DATA TRANSFER FROM
ANALOG-TO-DIGITAL CONVERSION
AND STORAGE BOARD TO A PC

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```
'PC DRIVER PROGRAM FOR DATA TRANSFER FROM THE ANALOG-TO-DIGITAL CONVERSION AND
'STORAGE BOARDS TO THE PC.

'IF YOU HAVE ANY QUESTIONS ABOUT THIS SOFTWARE PLEASE CONTACT:
'                          Thomas Kottke
'                          AMSRL-WT-WD
'                          Survivability Concepts Br.
'                          Weapons Concepts Div., Bldg 120
'                          Weapons Tech. Directorate
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'                          e-mail: kottke@arl.army.mil

'THIS CODE HAS BEEN WRITTEN FOR THE MicroSoft QuickBasic 4.5 PROGRAMMING
'ENVIRONMENT.

'*************************************************************************

DECLARE SUB DefineCNFGRegister ()  'this subroutine configures the National
                                   'Instruments PC-DIO-24 digital I/O board
                                   'that is used as the interface to the PC.

DIM NumBoards%(8), Value%(2047), BitPower%(8)

BaseAddress% = 2 * 256 + 1 * 16    'this base address matches the PC-DIO-24
                                   'base address that is selected using its
                                   'DIP switch array.

TimeLongPulse% = 300               'this variable defines the duration of the
                                   '"long" control pulse that is used to
                                   'reset the DTCB to initiate data transfer.

TimeShortPulse% = 1                'this variable defines the duration of the
                                   '"short" control pulses which signal the
                                   'DTCB to send the next data bit.

TimeSettle% = 3                    'this variable defines the duration of a
                                   'short delay which allows the DTCB time to
                                   'provide the next data bit.

ColorAxis% = 15                    'this variable defines the color that is
                                   'used to draw the axes on the PC monitor.

ColorGrid% = 8                     'this variable defines the color that is
                                   'used to draw the grid on the PC monitor.

FOR I% = 0 TO 7                    'the appropriate power of two is
    BitPower%(I%) = 2 ^ I%         'calculated for each bit position.
    NEXT I%

OUT BaseAddress% + 3, 2 * (Bank% + 4) + 1   'the control bit from the PC is
                                            'set high. due to the inversion
                                            'by the fiber optic receiver
                                            'this will result in a low PC OUT
                                            'signal at the DTCB.

CALL DefineCNFGRegister            'the PC-DIO-24 I/O board is activated.

CLS                                'the PC monitor screen is cleared.

LOCATE 5, 30                       'the software title is displayed and the
```

```
COLOR 11                                'user is asked to input the type of data
PRINT "PC DATA TRANSFER PROGRAM"        'transfer that they desire.
COLOR 3
LOCATE 15, 22
PRINT "Do you wish to  A) view data as a collection of data points"
LOCATE 17, 22
PRINT "                B) view data as a curve"
LOCATE 19, 22
PRINT "                C) transfer data to the PC hard disk"
LOCATE 21, 22
PRINT "                D) view and transfer data"
LOCATE 23, 22
INPUT "Input A, B, C or D:"; Ans1$

CLS                                     'the PC monitor screen is cleared.

                                        'if data is to be stored on the PC hard
                                        'drive, a datafile prefix is input.

IF ((Ans1$ = "C") OR (Ans1$ = "c") OR (Ans1$ = "D") OR (Ans1$ = "d")) THEN
    INPUT "Enter a test identification label (4 character maximum):"; File$
    END IF
PRINT : PRINT

                                        'the number of data acquisition banks is
                                        'input.

INPUT "Enter the number of data acquisition banks: "; NumBanks%
PRINT

                                        'the number of data acquisition boards is
                                        'input for each bank.

FOR Bank% = 0 TO NumBanks% - 1
    PRINT
    PRINT " Enter the number of data acquisition boards in bank"; Bank%; ":";
    INPUT NumBoards%(Bank%)
    NEXT Bank%

SCREEN 12                               'graphics screen is initialized and the
WINDOW (-100, -20)-(2050, 280)          'boundary values defined.

FOR Bank% = 0 TO NumBanks% - 1
    CLS
    LOCATE 1, 1
    PRINT "BANK:"; Bank%                            'print bank number.
    LINE (0, -1)-(2047, -1), ColorAxis%             'draw plotting axes.
    LINE (-1, 0)-(-1, 255), ColorAxis%
    FOR I% = 400 TO 2047 STEP 400                   'draw plotting grid.
        LINE (I%, 0)-(I%, 255), ColorGrid%
        NEXT I%
    FOR J% = 32 TO 255 STEP 32
        LINE (0, J%)-(2047, J%), ColorGrid%
        NEXT J%
    IF (Bank% = 0) THEN ANDMask% = 1                'define which I/O bit the data
    IF (Bank% = 1) THEN ANDMask% = 2                'will be transferred along.
    IF (Bank% = 2) THEN ANDMask% = 4
    IF (Bank% = 3) THEN ANDMask% = 8
    FOR Board% = 0 TO NumBoards%(Bank%) - 1         'define the color that each
        SELECT CASE Board%                          'board's data will be plotted
            CASE 0                                  'in.
                ColorData% = 3
            CASE 1
```

```
        ColorData% = 9
    CASE 2
        ColorData% = 10
    CASE 3
        ColorData% = 11
    CASE 4
        ColorData% = 12
    CASE 5
        ColorData% = 13
    CASE 6
        ColorData% = 14
    CASE 7
        ColorData% = 15
    END SELECT
LOCATE 2, 10 * Board% + 1              'print out the current board
COLOR ColorData%                       'value in the same color that
PRINT "Board"; Board%                  'the corresponding data is
COLOR 7                                'plotted in.

                                       'obtain the first byte of data.
                                       'the control signal for the
                                       'first bit of this byte must be
                                       '"long". all subsequent control
                                       'pulses must be "short".

Value%(0) = 0
FOR Bit% = 0 TO 7
    IF ((Board% = 0) AND (Bit% = 0)) THEN
        OUT BaseAddress% + 3, 2 * (Bank% + 4)        'generate a long
        FOR T% = 0 TO TimeLongPulse%: NEXT T%        'control pulse.
        OUT BaseAddress% + 3, 2 * (Bank% + 4) + 1
        ELSE
        OUT BaseAddress% + 3, 2 * (Bank% + 4)        'generate a short
        FOR T% = 0 TO TimeShortPulse%: NEXT T%       'control pulse.
        OUT BaseAddress% + 3, 2 * (Bank% + 4) + 1
        END IF
    FOR T% = 0 TO TimeSettle%: NEXT T%               'allow time for
                                                     'the DTCB to
                                                     'respond.

                          'because of the inversion by the fiber
                          'optic receiver, the data byte value is
                          'increased by the appropriate power of
                          'two if the transmitted bit value has a
                          'value of "0".

    IF (((INP(BaseAddress% + 2)) AND (ANDMask%)) = 0) THEN
        Value%(0) = Value%(0) + BitPower%(Bit%)
        END IF
    NEXT Bit%

                          'the same procedure is followed for the
                          'remaining 2047 data bytes on the active
                          'board except that it is assumed that all
                          'control pulses will be "short".

FOR Memory% = 1 TO 2047
    Value%(Memory%) = 0
    FOR Bit% = 0 TO 7
        OUT BaseAddress% + 3, 2 * (Bank% + 4)        'generate a short
        FOR T% = 0 TO TimeShortPulse%: NEXT T%       'control pulse.
        OUT BaseAddress% + 3, 2 * (Bank% + 4) + 1
        FOR T% = 0 TO TimeSettle%: NEXT T%           'allow time for
```

```
                                                        'the DTCB to
                                                        'respond.

                                    'because of the inversion by the fiber
                                    'optic receiver, the data byte value is
                                    'increased by the appropriate power of
                                    'two if the transmitted bit value has a
                                    'value of "0".

                IF (((INP(BaseAddress% + 2)) AND (ANDMask%)) = 0) THEN
                    Value%(Memory%) = Value%(Memory%) + BitPower%(Bit%)
                    END IF
                NEXT Bit%
            PSET (Memory%, Value%(Memory%)), ColorData%         'the transferred
                                                                'data value is
                                                                'plotted.
            NEXT Memory%

                                    'connect the data points with a line if
                                    'requested.

        IF ((Ans1$ = "B") OR (Ans1$ = "b")) THEN
            FOR Memory% = 2 TO 2047
                LINE (Memory% - 1, Value%(Memory% - 1))-
          (Memory%,Value%(Memory%)),ColorData%
                NEXT Memory%
            END IF

                                    'save the transferred data on the PC hard
                                    'disk if requested.

        IF ((Ans1$="C") OR (Ans1$="c") OR (Ans1$="D") OR (Ans1$="d")) THEN
            OPEN "C:\QB45\CAPMON\" + File$ + "_" + MID$(STR$(Bank%), 2, 1) +
                    "_" + MID$(STR$(Board%), 2, 1) + ".dat" FOR OUTPUT AS #1
            FOR Memory% = 0 TO 2047
                PRINT #1, Value%(Memory%)
                NEXT Memory%
            PRINT #1, "Date: ", DATE$     'stamp the datafile with the date...
            PRINT #1, "Time: ", TIME$     'and time.
            CLOSE #1
            END IF
        NEXT Board%

    BEEP                            'signal the end of data transmission for
    DO                              'this bank and suspend further transfer
        LOOP WHILE INKEY$ = ""      'until user acknowledges.

    NEXT Bank%

SUB DefineCNFGRegister

    SHARED BaseAddress%

    D7 = 1  'mode set
    D6 = 0  'mode "0"
    D5 = 0  'mode "0"
    D4 = 1  'port A input
    D3 = 0  'port C high nibble output
    D2 = 0  'mode "0"
    D1 = 1  'port B input
    D0 = 1  'port C low nibble input

    D% = D0 + D1 * 2 + D2 * 4 + D3 * 8 + D4 * 16 + D5 * 32
```

```
    D% = D% + D6 * 64 + D7 * 128
    OUT BaseAddress% + 3, D%
END SUB
```

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APPENDIX B:

MICROCONTROLLER DRIVER SOFTWARE FOR DATA TRANSFER
FROM ANALOG-TO-DIGITAL CONVERSION AND
STORAGE BOARDS TO A PC

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```
; 16C55 MICROCONTROLLER DRIVER PROGRAM FOR DATA TRANSFER FROM THE ANALOG TO
; DIGITAL CONVERSION AND STORAGE BOARDS TO THE PC.

; IF YOU HAVE ANY QUESTIONS ABOUT THIS SOFTWARE PLEASE CONTACT:
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; THIS CODE HAS BEEN WRITTEN FOR ASSEMBLY BY MICROCHIP TECHNOLOGY MPALC
; MACRO ASSEMBLER.

; ***************************************************************************

; REGISTER ALLOCATION

;  F08: counter for control signal classification
;  F09: denotes control signal classification
;  F0A: index for active analog-to-digital conversion and storage board
;  F0B: least significant byte of the active memory location index
;  F0C: most significant byte of the active memory location index
;  F0D: index for data byte bit position
;  F0E: latch register for memory data

; ***************************************************************************

; MACRO LIBRARY

;     Macro
;     Name                          Description
;  ------------   ------------------------------------------------------------
;  SetTRIS        determines the I/O port bit directions
;  SetOption      configures OPTION register to maximize time between timeouts
;  Classify       classifies control signals by their duration
;  ClearCounter   clears 744040 address generation counter
;  Reset          resets control board for data transfer
;  Standby        places control board in benign standby mode
;  MemLatch       latches memory location data
;  IncrBitPos     increments bit position of latched memory data
;  IncrMemAdd     increments memory address
;  IncrBoard      increments the active data acquisition board

; ***************************************************************************

; DEFINE CONSTANT VALUES

TotNumBrds      EQU     0x01            ;define total number of data
                                        ;acquisition boards in this bank

; ***************************************************************************

; MACRO FOR DETERMINING THE DIRECTIONS OF THE BITS OF THE I/O PORTS ---------

SetTRIS         MACRO                   ;start of MACRO to set I/O directions
                                        ;0=output, 1=input
                MOVLW   b'1011'         ;port A I/O direction template
                TRIS    0x05            ;load port A TRIS register
```

```
                MOVLW   b'11000000'     ;port B I/O direction template
                TRIS    0x06            ;load port B TRIS register

                MOVLW   b'11111111'     ;port C I/O direction template
                TRIS    0x07            ;load port C TRIS register

                ENDM                    ;end of MACRO

; MACRO TO SET OPTIONS ----------------------------------------------------

SetOption       MACRO                   ;start of MACRO to set options

                MOVLW   b'111111'       ;OPTION definition to maximize
                                        ;interval between watchdog timeouts
                OPTION                  ;load W into OPTION register

                ENDM                    ;end of MACRO

; MACRO TO CLASSIFY CONTROL SIGNALS ---------------------------------------

Classify        MACRO                   ;start of MACRO to classify
                                        ;control signals
                LOCAL   RepClass        ;define local variable
                LOCAL   NoClass         ;  "      "     "

                CLRF    0x08            ;clear register 08h
                CLRF    0x09            ;clear register 09h

RepClass        INCFSZ  0x08            ;increment register 08h, is it zero?
                GOTO    NoClass         ;(no) go to NoClass
                MOVLW   0xFF            ;(yes) load W with FFh
                MOVWF   0x09            ;transfer W to register 09h
NoClass         CLRWDT                  ;clear watch dog timer
                BTFSC   0x05,3          ;has PC OUT dropped yet?
                GOTO    RepClass        ;(no) repeat timing loop
                NOP                     ;(yes) filler

                ENDM                    ;end of MACRO

; MACRO TO CLEAR 744040 ADDRESS GENERATION COUNTER ------------------------

ClearCounter    MACRO                   ;start of MACRO to clear counter

                BSF     0x06,4          ;set MR high to reset 744040 output
                NOP                     ;filler to allow settling time
                BCF     0x06,4          ;reset MR to complete counter reset

                ENDM                    ;end of MACRO

; MACRO TO RESET DATA TRANSFER CONTROL BOARD -------------------------------

Reset           MACRO                   ;start of MACRO to reset board

                MOVLW   b'101000'       ;template to a)disable local output
                                        ;            b)reset MR low
                                        ;            c)set CP high
                                        ;            d)set board address to 0
                MOVWF   0x06            ;output template to port B

                ClearCounter            ;call MACRO to clear 744040 counter

                CLRF    0x0A            ;clear index for active board
```

```
                CLRF    0x0B            ;clear memory location least sig. byte
                CLRF    0x0C            ;clear memory location most sig. byte
                CLRF    0x0D            ;clear bit location index

                ENDM                    ;end of MACRO

; MACRO TO PUT DATA TRANSFER CONTROL BOARD IN STANDBY MODE ------------------

Standby         MACRO                   ;start of MACRO to standby board

                CLRWDT                  ;clear watch dog timer
                SetTRIS                 ;call MACRO to set I/O port direction
                SetOption               ;call MACRO to set controller OPTION

                BSF     0x06,5          ;disable local output

                ENDM                    ;end of MACRO

; MACRO TO LATCH MEMORY LOCATION CONTENTS ----------------------------------

MemLatch        MACRO                   ;start of MACRO to latch memory data

                BCF     0x06,5          ;enable local output
                NOP                     ;filler to allow settling

                MOVF    0x07,0          ;move port C data to W register
                MOVWF   0x0E            ;store W in register 0Eh

                BSF     0x06,5          ;disable local output

                ENDM                    ;end of MACRO

; MACRO TO INCREMENT LATCHED MEMORY DATA BIT POSITION ----------------------

IncrBitPos      MACRO                   ;start of MACRO to increment bit pos.

                RRF     0x0E,1          ;rotate right through carry bit
                INCF    0x0D,1          ;increment bit position index

                ENDM                    ;end of MACRO

; MACRO TO INCREMENT THE MEMORY ADDRESS ------------------------------------

IncrMemAdd      MACRO                   ;start of MACRO to incr. memory add.

                BCF     0x06,3          ;reset CP low
                NOP                     ;filler to allow settling
                BSF     0x06,3          ;set CP high

                INCF    0x0B,1          ;incr least sig. mem. add. byte

                BTFSC   0x03,2          ;is zero bit set?
                INCF    0x0C,1          ;(yes) incr most sig. mem. add. byte
                NOP                     ;(no) filler

                ENDM                    ;end of MACRO

; MACRO TO INCREMENT THE ACTIVE BOARD INDEX --------------------------------

IncrBoard       MACRO                   ;start of MACRO to increment board

                INCF    0x06,1          ;increment port B output value
                INCF    0x0A,1          ;increment board index register
```

```
                ENDM                    ;end of MACRO

; ********************** BEGINNING OF SOURCE CODE **************************

                SetTRIS                 ;set I/O port directions
                SetOption               ;maximize interval between timeouts

StandLoop       Standby                 ;place control board on standby
                BTFSS   0x05,3          ;is PC OUT high?
                GOTO    StandLoop       ;(no) repeat StandLoop

                Classify                ;(yes) classify control signal

                MOVF    0x09,1          ;move register 09h into itself

                BTFSS   0x03,2          ;is register 09h 0?
                GOTO    ResetYes        ;(no) go to reset control board jump
                GOTO    ResetNo         ;(yes) do not reset control board

ResetYes        Reset                   ;call MACRO to reset control board

ResetNo         MOVLW   0x08            ;load W with the value 08h
                SUBWF   0x0D,0          ;subtract W from bit position index
                BTFSS   0x03,2          ;is the zero bit set?
                GOTO    BitIncr         ;(no) go to bit increment routine
                CLRF    0x0D            ;(yes) clear bit position register

                IncrMemAdd              ;increment memory add. and indices
                MOVLW   0x08            ;load W with the value 08h
                SUBWF   0x0C,0          ;subtract W from most sig. mem. byte
                BTFSS   0x03,2          ;is the zero bit set?
                GOTO    MemGet          ;(no) go to memory increment routine
                CLRF    0x0B            ;(yes) clear least sig. mem. byte
                CLRF    0x0C            ;clear most significant memory byte
                ClearCounter            ;clear 744040 address counter

                IncrBoard               ;increment board pointer bits & index
                MOVLW   TotNumBrds      ;load W with the total num. of boards
                SUBWF   0x0A            ;subtract W from board index
                BTFSS   0x03,2          ;is the zero bit set?
                GOTO    MemGet          ;(no) go to memory increment routine
                GOTO    StandLoop       ;(yes) data trans complete, standby

MemGet          MemLatch                ;latch new memory data
BitIncr         IncrBitPos              ;increment bit position
                BTFSS   0x03,0          ;is the carry value set?
                GOTO    ClrPCIN         ;(no) go to reset PC IN routine
                BSF     0x05,2          ;(yes) set PC IN output line
                GOTO    StandLoop       ;repeat StandLoop
ClrPCIN         BCF     0x05,2          ;reset PC IN output line
                GOTO    StandLoop       ;repeat StandLoop

                END                     ;end of source code
```

LIST OF ABBREVIATIONS

ADC	analog-to-digital converter
ADCCB	analog-to-digital conversion calibration board
ADCSB	analog-to-digital conversion and storage board
DASCB	data acquisition and storage control board
DIP	dual inline parallel
DTCB	data transfer control board
LED	light-emitting diode
op amp	operational amplifier
PC	personal computer
PCFOCB	personal computer fiber optic communication board
RAM	random access memory

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